A Technique to Reduce Power and Test Application Time in BIST

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***Abstract*— Increased switching activity during testing causes substantial increase in power dissipation. This paper presents an efficient test application procedure for reducing power dissipation in test-per-scan BIST as well as the test application time, while maintaining the fault coverage. Experiments on ISCAS89 benchmarks show promising results - up to 51.8% (63.1%) peak power reduction and an average energy saving of 36.3% (62.3%) in the combinational logic (scan chain) for three partitions.**

I. Introduction

Power dissipation during test mode can be significantly higher than during functional mode, since the input vectors during functional mode are usually strongly correlated compared to statistically independent consecutive input vectors during testing.

Several approaches to reduce average power dissipation during test application have been proposed [1] [2]. They have either significant overhead in terms of test application time/area [1] or they are not computationally efficient or are test vector dependent [2] and, hence, are not suitable for large BIST circuits using weighted random patterns. Methods to reduce peak power dissipation has been mentioned in [3] - [7]. However, these methods do not guarantee prevention of peak power at all times [3] [4].

In this paper, we present a simple and efficient technique to reduce peak power as well as total energy dissipation during test application in scan-BIST. It involves modification of the scan architecture with additional DFT logic. The overhead is, however, far outweighed by the savings in the peak power during scan testing. We also present a novel test application procedure to reduce test application time and total energy dissipation while maintaining the fault coverage.

The rest of the paper is organized as follows: Section II presents the modified scan architecture and describes the proposed test application procedure in details. Experimental results are presented in Section III for a set of ISCAS89 benchmark circuits. Section IV concludes the paper.

II. Proposed Solution

A. Modified Scan Architecture

In this section, we describe the proposed test application procedure and the scan architecture to reduce the peak power dissipation. Fig. 1 shows the modified scan architecture suitable for the proposed test application. The basic idea is to split the scan chain and the primary inputs into multiple partitions and to allow only one partition to make transition

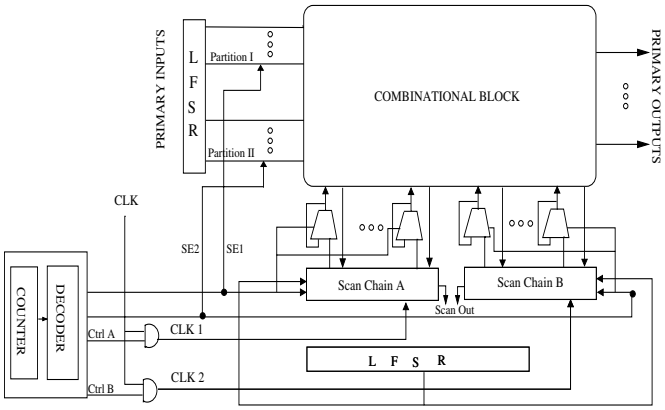

Fig. 1. Modified scan architecture for power reduction

at a time. Since switching is restricted to the fanout cone of the active scan chain, we restrict the number of simultaneous transitions in the circuit, thus, saving peak power. During shift cycles, only one partition of the scan chain loads in new scan-in values and shifts out previous state outputs. The other partitions of the scan chain remain disabled and do not incur any transition. Hence, rippling of scan transition is limited to only one partition, in contrast to rippling through the complete scan chain in conventional case. Since only one of the scan partition is active during shifting, we can disable the clock in other partitions, saving clock power significantly.

Prevention of switching in the combinational logic is very crucial and methods to tackle this problem has been mentioned in [5]. In the proposed scheme, we add a multiplexer at the output of the scan cells to prevent redundant switching of the combinational logic during shift cycle. This adds to area overhead and performance degradation. Assuming two transmission gates is required to implement the multiplexer, it leads to area increase of scan flop by 20%. This is comparable to the overhead incurred in [7].

We propose to use separate capture cycles for each scan partitions. It can be noted that the signature analyzer of the BIST is required to appropriately concatenate scan-out sequence received from the scan-out ports of different partitions before signature comparison.

Although, the maximum instantaneous power in combinational part is reduced, average power in the combinational logic can increase due to redundant switching in some gates. Since different partitions of primary inputs make transitions

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TABLE I

PEAK POWER REDUCTION USING THE PROPOSED TECHNIQUE

ISCAS89 circuit	% saving in comb logic		% saving in scan (shift)		% saving in scan (capture)	
	k=2	k=3	k=2	k=3	k=2	k=3
s5378	19.4 (35.9)	15.6 (48.5)	43.2	58.3	38.7	52.6
s9234	22.3 (38.9)	18.3 (49.9)	41.8	54.4	43.1	53.1
s15850	21.1 (26.45)	16.3 (43.2)	46.8	61	45.6	62.3
s35932	26.5 (32.4)	19.5 (50.5)	38.7	52.2	51.2	56.2
s38417	24.2 (43.3)	20.6 (51.8)	51.4	63.1	52.8	59.4
s38584	29.3 (33.1)	21.3 (51.4)	49.6	62.2	49.5	61.2
Avg.	23.8(35)	18.6(49.2)	45.25	58.6	48.8	57.4

TABLE II

ENERGY SAVING IN SCAN, COMBINATIONAL PART AND CLOCK LINE

ISCAS89 circuit	% saving in scan chain		% saving in comb logic		% saving in clock line	
	k=2	k=3	k=2	k=3	k=2	k=3
s5378	47.8	59.6	28.4	32.1	63.4	78.3
s9234	48.2	58.2	36.1	42.3	64.4	79.4
s15850	52.3	61.3	12.3	19	65.9	82.6
s35932	40.6	56.7	40.8	45.8	62.1	77
s38417	52.2	69.2	33.7	40.7	61.5	75.6
s38584	51.4	68.8	31.2	37.8	58.6	75.7
Avg.	48.75	62.3	30.4	36.3	62.6	78.1

at different times, there can be a region of overlap, which is sensitized by more than one partitions. Number of redundant switching tends to increase with more number of partitions because more number of gates fall into the overlapped region.

B. Reduction of Test Application Time

The proposed technique also has the potential to reduce test length (time). After one partition of the scan chain (partition A) is loaded with the new state input values (and the previous state responses scanned out), we start loading the other partition (partition B). While partition B is loaded with the new values, we perform a response analysis of the scanned out values from the partition A. After partition B is completely filled with new values, we check the result from the response analyzer of previous analysis. If positive result is achieved, we propagate the new state input values from partition B and the previous state output values from partition A. This is possible because the multiplexer at the output of the scan flop continues to propagate the old state output values to the combinational logic. Since this is a new state (previous state values in one partition and new scanned in state values in another partition), we use it to activate new faults and observe the response only at primary outputs. We then propagate the new scanned values of partition A and use it to detect new faults as in the conventional case. Thus the intermediate state can be used to detect new faults at the primary outputs. Hence, a new seed for the LFSR can be found such that if the LFSR is started from the new position, less number of tests is required to be applied to the circuit for the same fault coverage. We use a simple binary-search based algorithm to find the new seed for LFSR. With a reduced vector set, both test application time and total energy dissipation during test are improved.

III. EXPERIMENTAL RESULTS

To check the effectiveness of the proposed power saving technique, we performed simulations on a set of ISCAS89 benchmark circuits. Fault simulation and test vector set was generated using the tool Atlanta/Hope [8]. The proposed scan architecture was simulated for partition of the scan chain into two (k = 2) and three (k = 3) sets. *NanoSim* from Synopsys was used for power estimation.

The experimental results for the proposed technique for peak power reduction are summarized in Table I. It shows peak power improvement in both combinational part and scan chain when partitioned into two and three sets respectively.

Table II shows the total energy saving in the scan cells, combinational logic and clock line, using the proposed technique. Part of energy saving in the scan chain and clock line comes from intermediate response comparison at the primary outputs to reduce test application time. The energy saving in combinational logic is achieved by preventing logic propagation to the combinational part during scan shifting.

IV. CONCLUSIONS

This paper presents a test procedure and associated scan architecture to prevent peak power violation in scan-based BIST during shift and functional cycles. In the process, we also reduce test application time, power due to switching in the clock line and total energy dissipated during scan testing.

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