First Level Hold: A Novel Low-Overhead Delay Fault Testing Technique

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Abstract

This paper presents a novel delay fault testing technique, which can be used as an alternative to the enhanced scan based delay fault testing, with significantly less design overhead. Instead of using an extra latch as in the enhanced scan method, we propose using supply gating at the first level of logic gates to hold the state of the combinational circuit. Experimental results on a set of ISCAS89 benchmarks show an average reduction of 27% in area overhead with an average improvement of 62% in delay overhead and 87% in power overhead during normal mode of operation, compared to the enhanced scan implementation.

1 Introduction

With growing impact of process variation in sub-100nm technology regime, it is becoming mandatory for manufacturing test to include delay testing along with stuck-at tests [2]. Delay testing with *Enhanced scan* method allows application of arbitrary two-pattern test vectors at scan inputs for the best possible fault coverage [1] [4]. Enhanced scan method, however, involves high DFT overhead since it introduces an extra latch, named as hold latch, at the output of a scan flip-flop to hold the initialization pattern [4]. In this paper, we propose a novel delay fault testing technique, which allows enhanced scan-like test application, but comes at a much lower hardware overhead. The technique, referred as **First Level Hold** (**FLH**) employs the principle of "supply gating". Instead of holding the initialization pattern at the scan-hold latch [4], we hold the state of the combinational circuit in response to the first pattern by gating the VDD and GND of the first level gates. FLH does not require any extra control signal and does not change the test generation process. It does not affect fault models and eliminates redundant switching in the combinational block during scan shifting as in enhanced scan.

2 First Level Hold for Delay Fault Test

The basic idea is to use VDD and GND gating at the first level logic gates to prevent propagation of logic values to the combinational block. However, it makes the output of the first level gates floated and may not guarantee holding of state due to leakage variation, crosstalk noise and charge sharing between the floated output node and intermediate nodes. In order to ensure hold capability, we add a latch element (cross-coupled inverters) at the output node, as shown in Fig. 1(a). In the hold mode (TC='0'), the transmission gate is closed and the inverter loop holds the state of the output node. In the normal mode (TC='1'), however, the transmission gate is open and the gate can control its output. The proposed scheme is called "First Level Hold (FLH)" since only the first stage is set in the hold mode. The inverters (INV1 and INV2) and the transmission gate can use minimum-sized transistors to minimize their impact on area, circuit delay, and power during normal mode of operation.

Fig. 1(b) shows the proposed FLH technique applied to a general sequential circuit. FLH does not require any extra timing control signals. It uses the test control (TC) signal and its complement ($\bar{TC}$). The timing diagram during test application is shown in Fig. 1(c). During scan-in, TC is set to '0' to prevent activity in the scan chain affecting the combinational circuit. Once scan-shifting is completed for the first pattern (V1), it is applied to the combinational circuit by turning the gating transistors on, while the primary input (PI) bits are applied to PI. After the combinational circuit stabilizes, the second pattern (V2) is scanned-in while V1 is held since the gating transistors in the first level gates are turned off. Next, the transition is launched by activating TC and applying the PI bits and the results are latched after one rated clock period. As opposed to the enhanced scan, FLH does not require any "HOLD" signal.

3 Experimental Results and Comparisons

We simulated a set of ISCAS89 benchmark circuits and obtained area, power, and performance overhead in case of enhanced scan and FLH. The netlists were first technology-mapped to the *LEDA* 0.25μm standard cell library using Synopsys design compiler and then scaled to 70nm BPTM technology [6]. We assumed full-scan

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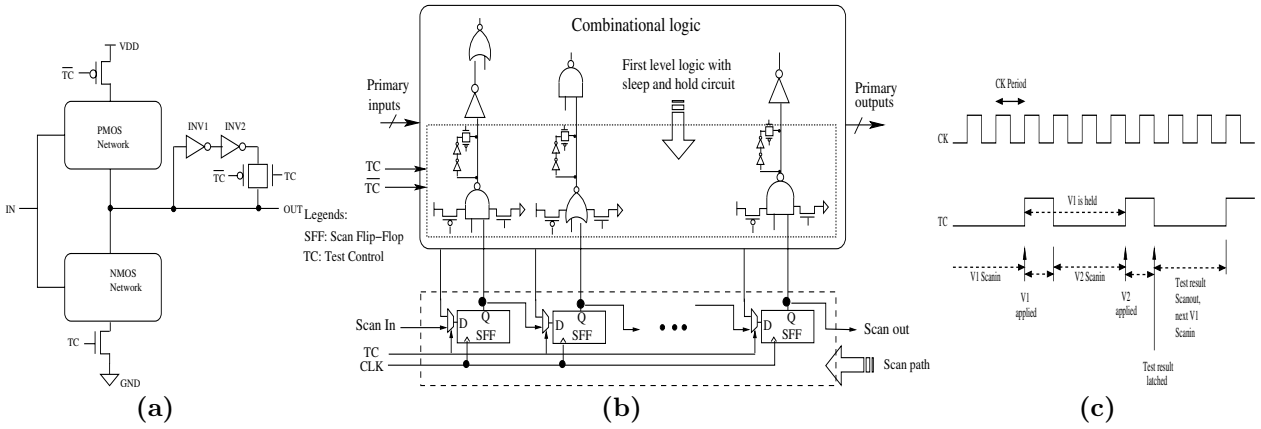

Figure 1. (a) Proposed supply gating scheme with output hold capability (b) Modified scan architecture with first level holding; (b) Timing diagram for delay testing with FLH

implementation of the benchmarks. Power is measured in *NanoSim* by applying 100 random vectors to the inputs and delay is measured by *Hspice* simulation of the critical path of a circuit. Table 1 shows comparison between two techniques. Since the layout rules for the 70nm node are not available, the measure used for area is the total transistor active area ($W * L$ for a transistor). FLH shows 27% reduction in area overhead (column 5) on an average as compared to enhanced scan. Compared to delay overhead in enhanced scan, an average improvement of 62% (column 6) is observed with FLH. As shown in the last column, the percentage reduction in power overhead is 87% on an average. This is because in FLH, the supply gating transistors do not switch in the normal mode. The only source of power overhead is due to switching of the minimum-sized inverters and the diffusion capacitance added to the outputs of first level logic by the transmission gate.

Table 1. Comparison of area, delay, and power between enhanced scan and FLH

ISCAS89 circuit	# Flip-flops	First level gates	Critical path logic levels	% improvement over enhanced scan		
				in Area	in Delay	in Power
S298	14	35	8	7.28	66.54	76.92
S344	15	32	11	20.88	52.67	86.05
S641	19	19	22	62.91	50.92	90.34
S838	32	96	20	-11.27	63.52	70.80
S1196	18	23	16	52.61	71.26	95.96
S1423	74	160	46	19.81	55.83	96.68
S5378	179	280	13	41.98	65.21	93.45
S9234	211	445	16	21.78	68.39	88.87

4 Conclusions

This paper presents First Level Hold (FLH), a novel technique based on supply gating, as a low-cost alternative to enhanced scan approach of delay fault testing. FLH is more suitable for high-speed applications since it induces significantly less delay in critical path of a circuit. At the same time, it provides the benefit of lower overhead in die-area and power consumption in normal mode of circuit operation, while not affecting test generation and application.

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