A High Performance IDDQ Testable Cache for Scaled CMOS Technologies

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Abstract

Quiescent supply current (IDDQ) testing is a useful test method for static CMOS RAM and can be combined with functional testing to reduce total test time and to increase reliability. However the sensitivity of IDDQ testing deteriorates significantly with technology scaling as intrinsic leakage of CMOS circuits increases. In this paper, we use a design technique for high-performance cache, which greatly improves leakage current and hence the IDDQ testability of the cache with technology scaling. We utilize the concept of Gated-Ground [1, 2] (NMOS transistor inserted between ground line and SRAM cell) to achieve reduction in leakage energy due to stacking effect of transistor without significantly affecting performance. Simulation results for a 64K cache shows 20% average improvement in IDDQ sensitivity for TSMC 0.25μm technology, while the improvement is more than 1000% for 70nm predictive technology model [12].

1. Introduction

IDDQ testing has been established as an effective technique [3, 4, 6, 7, 9, 10] to test CMOS SRAMs for realizing highly reliable systems. IDDQ testing is based on determining the quiescent supply current and can be used for burn-in elimination and for identifying issues related to yield and reliability [6, 14, 15]. Many defects, which do not generate any effect on output values of a memory cell and hence, cannot be modeled as functional faults, may be detected by IDDQ testing [3, 7]. Hence, few IDDQ vectors can be used effectively in memories to weed out some latent or reliability defects before applying functional testing [6, 7].

As transistor threshold voltage (V_{th}) is aggressively scaled at each technology generation to achieve high performance, sub-threshold leakage increases exponentially. It reduces the effectiveness of the IDDQ testing in CMOS circuits. Measuring the change in quiescent supply current between faulty and non-faulty circuit becomes increasingly difficult with technology scaling due to presence of elevated background leakage [13, 14, 15]. Many leakage control techniques have been proposed until now, however most of them need either complex process changes (like dual-V_{th} techniques) or change in test environment (like temperature changes), which are difficult to realize in practice [15].

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In this paper, we use a technique called *gated-ground* to reduce leakage in CMOS SRAM cache, thereby increasing IDDQ test sensitivity. *Gated-ground* technique was proposed in [1, 2] as a simple technique to achieve low power high performance SRAM that can be used in L1, L2 and L3 caches of a microprocessor. It uses stacking effect of transistors [5, 11] to reduce the sub-threshold leakage by inserting an NMOS transistor between the pull-down transistors of SRAM cell and the ground line. The extra NMOS transistor inserted, referred as *gated-ground* transistor, is shared among all the cells in a row and is turned off when the row is not accessed. Experiments show that the new cache named as DRG (Data Retention Gated-ground) cache, retains data when the *gated-ground* transistor remains off and consumes significantly low leakage energy with negligible performance loss of [1]. The area overhead in DRG-cache for the extra gated-ground transistor is merely 4% of the total cache area in a 64K L1 cache. A test chip is fabricated for a 2K DRG-cache for TSMC 0.25μm process technology and the experimental results from the chip verified that DRG-cache is a fully functional cache establishing the *gated-ground* technique a feasible approach.

We have modified the cache architecture proposed in [1] to make it suitable for IDDQ testing and analyzed the effectiveness of IDDQ testing in DRG-cache for current and future technologies. Since the stacking effect is expected to improve with technology scaling [11], the improvement in sub-threshold leakage and hence the IDDQ testability for DRG-cache are expected to enhance with technology. Simulation results from a 64K DRG-cache shows that IDDQ testing has much greater sensitivity in current technology while the sensitivity improves significantly for future technology generations.

The rest of the paper is organized as follows. Section 2 presents some of the previous works on IDDQ testing for CMOS SRAMs. Section 3 gives an overview of the circuit, architecture and layout of DRG-cache. Section 4 deals with details of IDDQ testing in DRG-cache. Section 5 presents simulation results for a 64K cache. Section 6 addresses some important test issues and section 7 concludes the paper.

2. Previous work on IDDQ testing in SRAM

Meershoek et al. [7] investigated the effectiveness of IDDQ testing in detecting defects in SRAMs. They compared IDDQ testing to traditional method of functional testing for an 8KX8 static RAM produced by Philips. Their experiments showed the relevance of IDDQ testing

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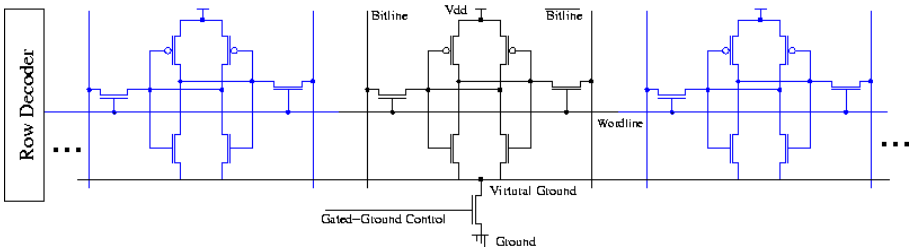

Figure 1. Anatomy of DRG-Cache: Data Retention Gated-Ground Cache

for product engineering due to its ability to detect majority of the functional faults and also some faults in the periphery, which do not show up as a functional error.

M. Hashizume et al. [3] examined if faulty CMOS SRAM ICs, which cannot produce the expected outputs, can be detected by measuring quiescent power supply current generated during write operation. They demonstrated that write cycle supply current is in the range of mA, which can be easily measured by test equipment. They also showed that it has better fault coverage than conventional IDDQ or functional testing.

Segura et al. [4] made a detailed analysis of IDDQ testability of gate oxide shorts (GOS) in CMOS SRAMs. They showed that IDDQ is effective in detecting GOS defects while the fault coverage of logic testing is limited. Their results also demonstrated the advantage of IDDQ testing over logic testing in detecting GOS defects in SRAMs. Soden [6] reported a qualification program for a 256K SRAM circuit using extensive IDDQ testing. The qualification program was able to identify several yield and reliability problems.

Champac et al. [9] addressed the detection of open defects in CMOS SRAMs observing IDDQ. They devised two techniques to detect open defects in SRAMs by forcing an initial condition during write cycle and by controlling the power supply level in conjunction with sequential accesses. They reported efficient detection of open defects with IDDQ testing using one or more IDDQ measurements.

Since IDDQ testing has been considered as an effective technique for detection of faults in CMOS SRAMs, a method to sustain its applicability for scaled technologies would have an important impact. In this paper we have analyzed a design technique to increase the sensitivity of IDDQ testing in CMOS SRAMs for present and future technologies by reducing sub-threshold leakage.

3. DRG-Cache: An overview

To prevent the leakage energy dissipation in a DRG-Cache from limiting aggressive threshold-voltage scaling, we use a circuit-level mechanism called *gated-ground* [1, 2]. *Gated-ground* enables a DRG-Cache to effectively turn 'off' the supply voltage and virtually eliminate the leakage energy dissipation in the cache's unused (used section of the cache core is defined as the SRAM cells from which data is read/written) sections. The key idea is to introduce an extra NMOS transistor (Figure 1) in the leakage path from the supply voltage to the ground of the cache's SRAM cells; The extra transistor is turned 'on' in the used and turned 'off' in the unused sections, essentially "gating" the cell's supply voltage. *Gated-ground* maintains the performance advantages of lower supply and threshold voltages while reducing the leakage. Figure 1 shows the anatomy of DRG-Cache. *Gated-ground* SRAM achieves significantly lower leakage because of the two off transistors connected in series reducing the leakage current by orders of magnitude; this effect is due to the self reverse-biasing of stacked transistors, and is called the stacking effect [11].

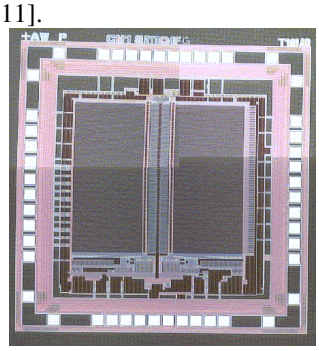

Figure 2. Die Photo of DRG-Cache

Figure 2 shows the die photo of the fabricated DRG-cache along with a conventional cache (to the left) for comparison. The rightmost thin column in layout is the *gated-ground* transistor. To minimize the area overhead and optimize layout, we implemented *gated-ground* transistor as rows of parallel transistors placed along length of the SRAM cells. This row of parallel transistor is placed at one end of row of SRAM cells. From the layout, the area overhead due to *gated-ground* transistor is about 4%. It is important to note that the DRG-Cache core is fully compatible with current cache design.

Figure 3 shows a single cell schematic of the DRG-Cache. When the *gated-ground* transistor is on, it behaves exactly like conventional SRAM in terms of storing data. Turning 'off' the gated-ground nicely cuts-off the leakage path from the cell node that is at '1' to ground. As the same time, it also cuts-off the opportunity to strap the cell node at '0' firmly to ground. This makes it easier for a noise source to write a '1' to that node. Node storing '1' remains firmly strapped to V_{dd} as long as input ($\overline{Q}$) to the pull-up PFET (M4) remains below the trip point of the inverter. However, the stability of a cell in the DRG-cache and its data retention capability were verified from

simulations of the netlist extracted from layout and also from experimental results from the fabricated chip.

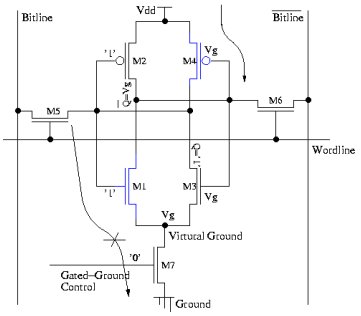

Figure 3. DRG-Cache: Data Retention Capability

In DRG-Cache, the *gated-ground* transistor can be controlled by the row decoder logic of conventional SRAMs or by introducing an extra decoder that decodes only some of the Most Significant Bits (MSB) of the row address. To make the DRG-cache IDDQ-testable, certain modifications are made which are discussed in section 4.

4. IDDQ testing for DRG-Cache

In IDDQ testing, the quiescent supply current (IDDQ) is measured for the Device Under Test (DUT). Since the quiescent current for a "good" CMOS circuit is very small, if an abnormally high IDDQ is detected for the DUT, it is determined to be faulty. Test techniques that monitor the IDDQ of CMOS circuits are effective to detect defects causing significant change in leakage [3, 4, 9, 10, 14]. For CMOS SRAM circuits, the defects which can be detected by IDDQ testing include most of the bridging defects which can be modeled as stuck-at fault (SAF) e.g. a bridge between V_{dd} to non-V_{ss} node or stuck-open fault (SOF) e.g. a bridge between V_{ss} to WL or coupling fault (CF) e.g. bridge between BL1 to BL2 [8]. IDDQ testing can detect some of the open defects in SRAM too e.g. opens in word line (WR) or in bit line (BL) (marked as A and B in figure 4), which can be modeled as data retention fault (DRF) [3]. Open defects in the drain (source) of transistors and floating gate defects behaving as stuck-open transistors are also detected by IDDQ testing [9]. Most of the defects in SRAMs covered by IDDQ testing can be classified as functional faults or logical faults i.e. they affect the output logic of a memory cell. However, IDDQ testing can also detect defects such as gate oxide shorts. These defects may not change the logic operation of the circuit in many cases [4] and hence cannot be detected by functional or logic testing methods.

Many defects detectable by the IDDQ testing, exhibits increased leakage only during a write operation. A write cycle can force most nodes to a specific voltage, which causes elevated IDDQ when shorted nodes are forced to different voltages [3, 7]. For the bit lines, p-channel pull-ups are used, which are not turned off in the write cycle and a large current in the range of mA is generated during the writing phase.

4.1. Measurement of IDDQ sensitivity

The effectiveness of an IDDQ testing method can be determined by the change in leakage current in a faulty device with respect to the leakage in a non-faulty one. The sensitivity of IDDQ testing can be computed using (1), which is proportional to the absolute difference in leakage between the faulty and fault-free device. Higher difference in leakage translates into higher sensitivity for detecting a fault. For scaled technologies leakage increases exponentially and hence sensitivity of IDDQ testing decreases.

$$Sensitivity = \frac{IDDQ(faulty) - IDDQ(nonfaulty)}{IDDQ(nonfaulty)} \quad (1)$$

The sensitivity measurement in (1) can be used as a metric to compare IDDQ testability in two different technologies. The percentage improvement in sensitivity in one IDDQ testing method compared to another method can be computed as in (2). We have used (1) and (2) to compare the effectiveness of DRG-cache with conventional 6-T cache.

$$improvement = \frac{Sens(method2) - Sens(method1)}{Sens(method1)} \times 100\% \quad (2)$$

4.2. Fault detection

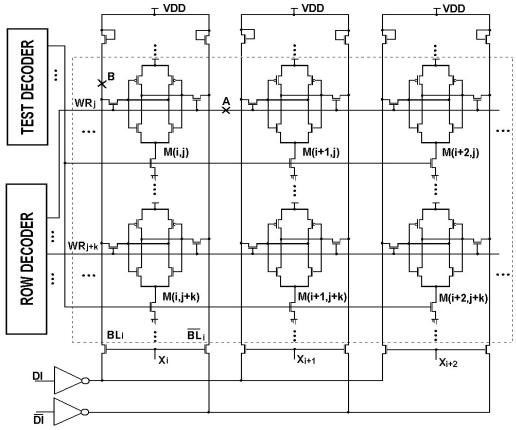

Figure 4. IDDQ Testable DRG-Cache Architecture

Fault detection in a DRG-cache using IDDQ testing can be done by incorporating simple modifications to the cache architecture as described in Figure 4. There is an extra decoder that decodes some of the MSBs of the row address (named as *Test Decoder*). The decoder output is connected to the gate of the *gated-ground* NMOS transistors. If *n* MSBs of the row address are used for the *Test Decoder*, there are 2^n outputs of the decoder to trigger the *gated-ground* transistors. Hence, rows of the cache can be divided into 2^n non-overlapping blocks, each having same address for the *n* MSBs. When a particular address of the cache is accessed for read/write, the *gated-ground* transistor for the entire block is turned on. This allows an abnormal supply current due to a defect in the block to

flow from V_{dd} to ground (except for a V_{dd} to V_{ss} bridge, which generates elevated leakage at all time).

Control signals for the *gated-ground* transistor can also be taken from output of the row address decoder i.e. from the WL lines (as done in [1]) instead of generating them by an extra decoder. But that may need more test cycles to activate and detect IDDQ testable faults.

5. Simulation results

A 64K DRG-cache was simulated with *Hspice* to determine its IDDQ testability for different defects and different technologies. Netlist of the cache is extracted from a layout implemented in TSMC 0.25µm process. Ten different bridging defects conforming to different fault classes [8] are chosen for simulation. Open defects in the drain of PMOS and NMOS transistors are also considered in the simulation.

IDDQ for the DRG-cache is measured during the write cycle. Data to be written to the defective cell is either '1' (for defect like V_{ss} to $Q/\overline{Q}$) or '0' (for defects like WL to $Q/\overline{Q}$). To activate a defect between two adjacent cells (e.g. a bridge between BL of one cell and Q of adjacent cell), different values ('0' for one cell and '1' for the other) are written into the cells.

Table 1 presents simulation results to compare IDDQ sensitivity (as computed in (1)) of DRG-cache with conventional cache. Sensitivity data and percentage improvement (computed as (2)) are presented for 6 different bridging defects with 3 different block sizes. The results correspond to TSMC 0.25µm technology with default V_{th} (0.45V). We get about 11% improvement in IDDQ sensitivity when block size is 1/2 the cache size. Sensitivity improvement is around 21% and 23% for block size of 1/8 and 1/16 of cache size respectively. The

Table 1. Sensitivity result for TSMC 0.25µm (V_{th}=0.45V)

Block Size	Bridge	Sensitivity with conv. cache	Sensitivity with DRG-cache	% Improve.
1/2	**vdd - q/qb**	37.14	39.73	**6.98**
	vss - q/qb	45.04	50.19	**11.42**
	bl1 - bl2	165.86	182.78	**10.20**
	bl -blb	138.82	153.71	**10.73**
	q - qb	26.91	29.46	**9.45**
	bl1 - q2	179.48	209.60	**16.78**
1/8	**vdd - q/qb**	37.14	43.67	**17.59**
	vss - q/qb	45.04	55.11	**22.35**
	bl1 - bl2	165.86	200.13	**20.66**
	bl -blb	138.82	168.34	**21.26**
	q - qb	26.91	32.44	**20.52**
	bl1 - q2	179.48	229.46	**27.85**
1/16	**vdd - q/qb**	37.14	44.38	**19.50**
	vss - q/qb	45.04	56.00	**24.33**
	bl1 - bl2	165.86	203.33	**22.58**
	bl -blb	138.82	171.03	**23.20**
	q - qb	26.91	32.97	**22.49**
	bl1 - q2	179.48	233.12	**29.88**

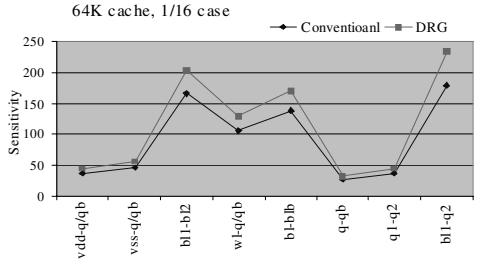

Figure 5. Sensitivity for conventional and DRG-cache (TSMC 0.25µm)

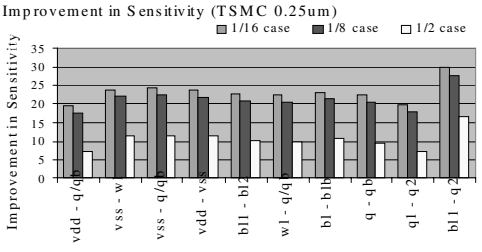

Figure 6. Improvement in sensitivity for different sizes (TSMC 0.25µm)

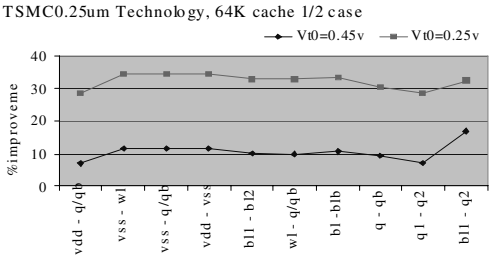

Figure 7. Improvement for different V_{th}, 1/2 case (TSMC 0.25µm)

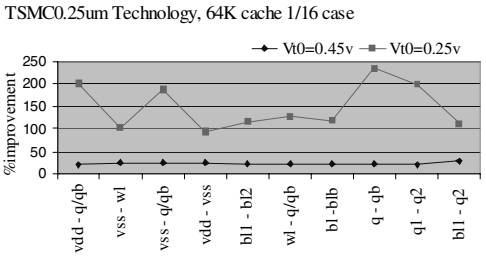

Figure 8. Improvement for different V_{th}, 1/16 case (TSMC 0.25µm)

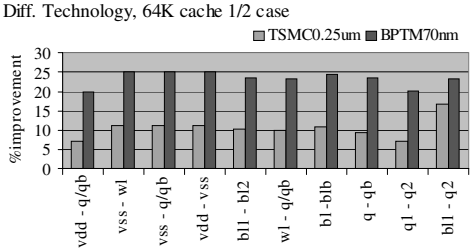

Figure 9. Improvement for different technologies

Table 2. Sensitivity result for V_{th}=0.25µm (TSMC 0.25µm)

Block Size	Bridge	Sensitivity with conv. cache	Sensitivity with DRG-cache	%Improve.
1/2	**vdd - q/qb**	0.80	1.03	**28.57**
	vss - q/qb	0.98	1.32	**34.50**
	bl1 - bl2	3.75	4.98	**32.88**
	bl -blb	3.28	4.37	**33.26**
	q - qb	0.63	0.82	**30.28**
	bl1 - q2	4.40	5.83	**32.34**
1/8	**vdd - q/qb**	0.80	2.20	**175.52**
	vss - q/qb	0.98	2.59	**164.57**
	bl1 - bl2	3.75	7.54	**100.97**
	bl -blb	3.28	6.71	**104.63**
	q - qb	0.63	1.92	**204.99**
	bl1 - q2	4.40	8.67	**97.04**
1/16	**vdd - q/qb**	0.80	2.40	**200.28**
	vss - q/qb	0.98	2.81	**187.22**
	bl1 - bl2	3.75	8.07	**115.03**
	bl -blb	3.28	7.18	**119.15**
	q - qb	0.63	2.10	**233.63**
	bl1 - q2	4.40	9.27	**110.61**

improvement we get for decreasing the block size from 1/8 to 1/16 of the cache size is much less than the improvement for decreasing it from 1/2 to 1/8. This is since the improvement in leakage decreases linearly with the number of rows in a block. The *Test Decoder* size increases as logarithm of the number of blocks, e.g. a *Test Decoder* of size 3X8 is required for block size of 1/8 of the cache size.

Figure 5 compares the IDDQ sensitivity of DRG-cache with conventional cache for different bridging defects. The plot corresponds to block size of 1/16 of the cache size. Plot for two defects are not shown because sensitivity for them is too high. Figure 6 plots the percentage improvement in sensitivity for three different block sizes as listed in Table 1.

Sensitivity for different block sizes is presented in Table 2 for TSMC 0.25µm technology with reduced V_{th} (0.25V) for the NMOS transistors (pull-down and *gated-ground* transistors). Improvement in sensitivity for two different V_{th} is plotted in Figure 7 and 8 for block size 1/2 and 1/16 of the cache size, respectively. Decreasing the V_{th} of the NMOS transistor helps improve the IDDQ sensitivity of DRG-cache as depicted in Figure 7 and 8.

Simulation results for 70nm Berkeley Predictive Technology Model (BPTM) [12] is presented in Table 3 for both the caches for different defects and different block sizes. V_{dd} used for this model is 1.0V and all device parameters are scaled according to the BPTM model. Figure 9 plots the percentage improvement in sensitivity for BPTM70nm compared to TSMC0.25µm for all the defects. For 70nm, we get average IDDQ sensitivity improvement of about 23%, 1946% and 2170% for block sizes 1/2, 1/8 and 1/16 of the cache, respectively. The improvement is large compared to 0.25µm technology. The trend of sensitivity improvement with decreasing

Table 3. Sensitivity results for BPTM70nm

Block Size	Bridge	Sensitivity with conv. cache	Sensitivity with DRG-cache	%Improve.
1/2	**vdd - q/qb**	0.0154	0.0185	**19.94**
	vss - q/qb	0.0184	0.0230	**25.13**
	bl1 - bl2	0.0695	0.0860	**23.75**
	bl -blb	0.0583	0.0725	**24.36**
	q - qb	0.0109	0.0135	**23.61**
	bl1 - q2	0.0768	0.0945	**23.03**
1/8	**vdd - q/qb**	0.0154	0.5646	**3559.63**
	vss - q/qb	0.0184	0.5702	**2995.65**
	bl1 - bl2	0.0695	0.6478	**832.21**
	bl -blb	0.0583	0.6311	**982.73**
	q - qb	0.0109	0.5584	**5015.57**
	bl1 - q2	0.0768	0.6583	**756.67**
1/16	**vdd - q/qb**	0.0154	0.6276	**3967.90**
	vss - q/qb	0.0184	0.6334	**3338.84**
	bl1 - bl2	0.0695	0.7141	**927.68**
	bl -blb	0.0583	0.6968	**1095.39**
	q - qb	0.0109	0.6212	**5590.30**
	bl1 - q2	0.0768	0.7251	**843.55**

Table 4. Sensitivity results for open defects (TSMC 0.25µm)

Cache size	Open defect location	Sensitivity with conv. cache	Sensitivity with DRG-cache	% Improve.
64K	**Pmos drain**	0.033	0.044	**31.26**
	Nmos drain	0.385	0.491	**27.31**
16K	**Pmos drain**	0.119	0.156	**31.11**
	Nmos drain	1.370	1.742	**27.16**
4K	**Pmos drain**	0.389	0.509	**30.88**
	Nmos drain	4.483	5.690	**26.94**

block size is similar to 0.25µm process due to reason mentioned earlier.

Sensitivity results for some IDDQ-testable open defects are given in Table 4 for different cache sizes. Technique described in [9] is used for testing the open defects. On an average, we get approximately 29% improvement in sensitivity for open defects using 0.25µm process. This demonstrates that DRG-cache is also superior to conventional cache for IDDQ testing of open defects.

6. Test issues

6.1. Effect of technology scaling

Sensitivity of IDDQ testing in DRG-cache greatly improves with technology scaling. This can be observed from simulation results in Table 3. Drain Induced Barrier Lowering (DIBL) effect in transistor increases with scaling which in turn causes increased self-reverse biasing of the *gated-ground* transistor resulting in improved stacking effect [11]. Improved stacking effect helps in reducing leakage that increases sensitivity for IDDQ testing. This observation makes DRG-cache very promising for sustaining the effectiveness of IDDQ testing in future technology generations.

6.2. Effect of gated-ground transistor size

Sharing the *gated-ground* transistor among multiple SRAM cells in a row amortizes the overhead of the extra transistor. Because the size of *gated-ground* transistor plays a major role in the data retention capability and stability of the DRG-Cache, and also affects the power and performance savings [1], the *gated-ground* transistor must be carefully sized with respect to the SRAM cell transistors it is gating. While the *gated-ground* transistor must be made large enough to sink the current flowing through the SRAM cells during a read/write operation in the active mode and to enhance the data retention capability of cache, too large a *gated-ground* transistor may reduce the stacking effect, thereby decreasing the test sensitivity. Moreover, large transistors also increase the area overhead.

6.3. Effect of transistor threshold

Transistor threshold voltage (V_{th}) of the *gated-ground* transistor has an impact on the IDDQ sensitivity of the DRG-cache. Table 2 shows that the improvement in sensitivity for DRG-cache for reduced V_{th} (0.25V) is about 7 times higher than the sensitivity for the default V_{th} (0.45V) for block size of $1/8^{th}$ of cache size. The increase in sensitivity for lower V_{th} can be attributed to the fact that stacking effect improves with lower V_{th}. It is important to note that even if the improvement in sensitivity increases for DRG-cache, absolute measure of sensitivity decreases exponentially for reduced V_{th} in both the caches. This is due to an exponential increase in leakage of non-faulty device with V_{th} scaling.

Voltage at node storing logic '0' gets saturated at lower value with lower V_{th} process. This is due to the fact that lowering the V_{th} increases the leakage current of all the transistors and since the discharging current is stronger than the charging current in the low V_{th} case, the saturation voltage is lower. Lower V_{th} improves stability but decreases the IDDQ testability because of increased background leakage.

6.4. Fault localization

The proposed IDDQ test methodology for DRG-cache has the advantage of localizing defects. This is particularly important for defects, which do not need to be tested during a write cycle. These defects cannot be localized in conventional cache. In a DRG-cache, these defects can be localized within a block since they are activated only when the *gated-ground* transistors of the block are turned on. The resolution of localization can be increased by decreasing the block size. This can be achieved at the expense of a larger *Test Decoder* and more complex routing of gating signals.

7. Conclusions

In this paper we propose a high performance low leakage testable cache (DRG-cache). Sensitivity of IDDQ testing of DRG-cache improves significantly with technology scaling since stacking effect is expected to improve with scaling. IDDQ sensitivity in a DRG-cache depends on the fraction of the total cache turned on during testing. However, this might have an impact on total IDDQ test time for the cache.

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