Ultralow-Power Reconfigurable Computing with Complementary Nano-Electromechanical Carbon Nanotube Switches

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Abstract

In recent years, several alternative devices have been proposed to deal with inherent limitation of conventional CMOS devices in terms of scalability at nanometer scale geometry. The fabrication and integration cost of these devices, however, have been prohibitive and/or the devices do not allow smooth transition from the conventional design paradigm. To address some of these limitations, we have developed a new family of devices called "Complementary Nano Electro-Mechanical Switches" (CNEMS) using carbon nanotubes as active switching/latching elements. The basic structure of these devices consists of three co-planar carbon nanotubes arranged so that the central nanotube can touch the two side carbon nanotubes upon application of a voltage pulse between them. Owing to the unique properties of carbon nanotubes, these devices have very low leakage current, low operation voltages, and have built-in energy storage to reduce computation power, resulting in very low overall power dissipation. CNEMS have stable on-off state and latching mechanism for non-volatile memory-mode operation. Besides, the devices can be readily integrated in the same substrate as CMOS transistors with high integration densities - thus, allowing easy manufacturability and hybridization with conventional CMOS devices. In this paper, we present the properties of these devices and based on our analysis, we propose a reconfigurable computation framework using these devices. For the first time, we demonstrate that these devices are promising in dynamically reconfigurable instant-on system development with about 25X lower power dissipation.

1. INTRODUCTION

While CMOS technology has served the semiconductor industry marvelously for the past four decades (by allowing nearly exponential increase in computational power and device integration density), it is predicted to meet the end of roadmap in near future due to the intrinsic physical limitations of the device in terms of scalability. At nanometer scale, CMOS devices suffer from increasing short channel effect [12] that results in high leakage current. High dynamic power and power density have also emerged as major barriers to gigascale integration. On the other hand, drain to source voltage (V_{DS}) reduces with scaling, while the series resistance increases, giving rise to reduced saturation current and I_{ON}/I_{OFF} ratio. Variations in manufacturing process parameters, such as length (L), width (W), threshold voltage (V_{TH}) have increased alarmingly with continued miniaturization of device geometry and supply/threshold voltage scaling. Hence, manufacturing yield and robustness of operation under severe process variations have manifested as major design concerns.

To address some of these issues, there has been multitude of research efforts to develop alternative devices with promising characteristics in terms of performance and/or integration density. Most of these emerging devices either demand prohibitive manufacturing costs or introduce a completely new paradigm of computing. However, to achieve a smooth transition from conventional MOSFET devices to a viable alternative at the end its roadmap, it is beneficial to have a potent technology, which allows system manufacturing by extending the existing CMOS fabrication and enables utilization of the rich repository of existing CAD tools.

In this paper, we present a new device called Complementary Nano Electro-Mechanical Switch (CNEMS) that uses carbon nanotube (CNT) [1-5, 10-11] as active element. Acting as a mechanical relay, the switch can be toggled between two complementary configurations by application of an electric field between two of its terminals. Once configured in a certain way, the switch remains in the same state until an opposite electric field is applied to reconfigure the switch. Due to this latching mechanism, *each switch works as a non-volatile memory element.* In a CNEMS, electron transport between two connected terminals is ballistic. Due to the electro-mechanical nature of the switch, there is virtually no leakage current between two terminals when they are not connected. Another important feature of the device is that, once it is programmed, certain amount of elastic energy remains internally stored in the carbon nanotubes, so that all subsequent reconfigurations of the switch require less electric field and thus less energy for transition. *This feature of internal energy storage [6-9] helps to reduce the active power of the switch considerably.*

Due to the unique properties of carbon nanotubes, these devices have very stable on-off states and low operation voltage. Since the CNEMS has low leakage, it has extremely high data retention capability. The device is also completely immune to soft error (e.g. memory failures due to alpha/neutron particle hit) [14], unlike CMOS based memory. Therefore, CNEMS is a good candidate for memory implementation and can potentially replace conventional charge-based CMOS static and dynamic RAM. Unlike the conventional CMOS logic circuits, which evaluates logic function based on charge stored in a node [12] (defined by the diffusion and or gate capacitances of the devices), the proposed CNEMS based logic evaluates in two steps: a) configure and then b) propagate logic value. In the "configure" step, the switch is programmed to select one of the two inputs and in the following "propagate" step, the switch propagates the right input to the output. We propose a reconfigurable computing framework using these devices. Since each CNEMS switch can be treated as a non-volatile memory element, we can use them in realizing lookup table (LUT) based logic circuits [13]. Compared to the conventional FPGA architecture, the proposed framework has the following

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advantages. a) The CNEMS switches used to build the lookup table can be configured as register banks or latches for storing data. It can be particularly helpful to improve performance in general purpose or digital signal processing, where an array of lookup tables can be used to configure either certain datapath element (e.g. an image encoder in a streaming application) or register banks (in a data-intensive application). b) The system developed with CNEMS, will be instant-on (due to non-volatile nature of the switches) unlike SRAM-based FPGA [13] and dynamically reconfigurable (due to fast transition of the states in the switches). c) The system can achieve ultra low power operation and reconfiguration and d) due to less "ON" resistance and non-volatility of these switches, they can be used in developing efficient low-power programmable switches.

2. DEVICE AND TECHNOLOGY

In this section, we present carbon nanotube [1-5] based electro-mechanical switches with internal energy storage as complementary or alternative to the existing CMOS switches in certain applications. Devices with internal energy storage were proposed by Feynman [6, 7] and Bennett [8, 9] for reduced power computation and bit processing. The main idea was that if one uses a spring as the computation device, the "one" state may be achieved by compressing the spring and latching it so that it does not spring back. Subsequently, in transitioning to the "zero" state, the stored energy in the compressed spring can be retrieved and re-used to reduce the energy per bit. With the discovery of carbon nanotubes and their applications in electronics [1-5, 10-11], we note that CNTs with their large Young's modulus (1.3 TPa) [10] and very small diameters (1-100nm), are ideal electronic device-grade "springs" for Feynman-Bennett type computation devices. Hence we propose to develop a very unique category of electronic devices with internal energy storage capacity and other desirable characteristics such as very low leakage and high transition speeds. The basic structure of the proposed complementary nano electro-mechanical switch (CNEMS) consists of three co-planar carbon nanotubes arranged so that the central nanotube can touch the two side carbon nanotubes upon application of a voltage pulse between them. When the central CNT touches one of the side CNTs, the van der Waals force causes them to "stick" to each other resulting in latching. The CNTs are then "unstuck" by applying a voltage between the central CNT and the third CNT on the opposite side. Certain amount of energy is stored in the elastic deformation of the CNT when it is bent to make contact with a side CNT. This energy becomes available when the central CNT is released and attracted to the opposite CNT. Noting that CNTs have very large Young's modulus of around 1.3 TPa, very fast CNEMS with sub-nanoseconds switching times can be realized provided that CNT lengths are kept below L<100nm that in turn requires precise CNT-CNT distances of around d_{cnt}< 50nm. The proposed CNEMS have very large on-to-off conductance ratio (>10^{12}), are radiation hard, and can be fabricated on CMOS circuits.

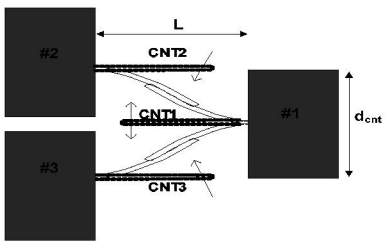


Figure 1. Complementary nano electro-mechanical switch (CNEMS). The central CNT (CNT1) is either touching the top (CNT2) or bottom (CNT3) one. Latching is caused by the van der Waal force and the energy stored in CNT1 is recovered when it is transitioned.

2.1. Device Characteristics

CNEMS characteristics critically depends on the kind of carbon nanotube we use, how close we place them near each other and the bottom electrode, and how long the carbon nanotubes are. As discussed next, carbon nanotubes can be single-walled (SWCNT) or multi-walled (MWCNT) depending on how they are grown and their growth temperature. The MWCNTs are usually metallic while SWCNTs can be both metallic and semiconducting. The gap distance between CNTs and a bottom electrode can be designed to be between 20-100nm. Smaller gaps will result in unwanted van der Wall clamping of the CNTs to the bottom surface while larger gaps will result in unacceptably larger "reset" voltage (V_r= reset voltage is the voltage needed to "un-stuck" all the CNTs from each other so that complete isolation can be achieved between different parts of the circuit.) It is desirable to have the CNT-CNT distance as small as possible because then the threshold voltage (V_{th}= voltage needed to attract adjacent CNTs together) can be made very small and the CNT length can be scaled down correspondingly increasing the transition speed (v_t). We discuss these parameters in detail below.

2.2 Device Operation Principles

To calculate the turn-on, or the threshold, voltage we note that the total energy of two adjacent CNTs is given by: $E_t = E_{vdW} + E_{elastic} + E_{electrostatic}$. The van der Waals interaction between CNTs has been calculated by researchers and lower bound to the expected attractive energy can be described using an empirical formula given by $E_{vdW} = (-0.053 + 0.086d)L$ eV, where "d" is the CNT diameter expressed in $\mathring{A}$ and L is the interaction length also in $\mathring{A}$. This empirical equation is only applicable when the CNTs are touching each other. When they are not, Leonard-Jones type of potentials that contain r^{-6} and r^{-12} CNT-CNT position (r) dependences can be used to calculate E_{vdW} as a function of distance. The elastic energy can be calculated using beam mechanics model and is given by: $E_{elastic} \sim 1.6\frac{\delta^2 EI}{L^3}$ where δ is the displacement of CNT's tip, E is the Young's modulus (~1.3 TPa for SWCNTs), and I is the moment of inertia ($=\frac{\pi}{64}[d_1^4 - d_2^4]$, where d_1 is the outer diameter of the CNT and d_2 is its inner diameter). The electrostatic energy is given by $E_{electrostatic} = \frac{1}{2}CV^2$ where C is the capacitance between two adjacent CNTs and V is the

applied voltage. Considering two CNT's symmetrically bending toward each other, the "C" can be approximated using a parallel cylinder capacitor with uniform distance d_{cnt}. It can be shown that $C \sim \frac{2}{3}\frac{\varepsilon_0 dL}{d_{CNT}}$. When the two CNTs touch each other, we have $\delta = d_{cnt}/2$.

Next we note that the electrostatic ($F_{electrostatic} = -\frac{\partial E_{electrostatic}}{\partial x}$) and van der Waals ($F_{vdW} = -\frac{\partial E_{vdW}}{\partial x}$) forces are both attractive while the elastic force ($F_{elastic} = -\frac{\partial E_{elastic}}{\partial x}$) is not. Thus, at $-\frac{\partial E_{total}}{\partial x} = 0$, the total forces acting on the CNTs cancel out and result in a stable configuration. When $F_{vdW} \geq F_{elastic}$ (V=0 V) the van der Waals forces overcome the elastic force and CNTs can latch onto each other. Clearly this situation should be achieved after application of a voltage pulse because otherwise, the CNTs' will spontaneously clamp onto each other. This simple but important observation puts a limit on how close CNTs can be to each other.

The above equations can be solved to study scaling laws of CNEMS and design devices with different feature sizes and characteristics. To demonstrate feasibility of switching and latching with reasonable voltages and device structures, we consider the CNEMS structure schematically shown in Fig. 1. Taking d_{cnt}~*20*nm, and *L=50*nm, and d_1~3nm, d_2~3.5nm, we calculate $E_{elastic}$~ *34* eV while E_{vdW}~*740* eV. The two energies are equal at L~19nm for d~3.5nm and d_{cnt} of 20nm (δ~10nm).

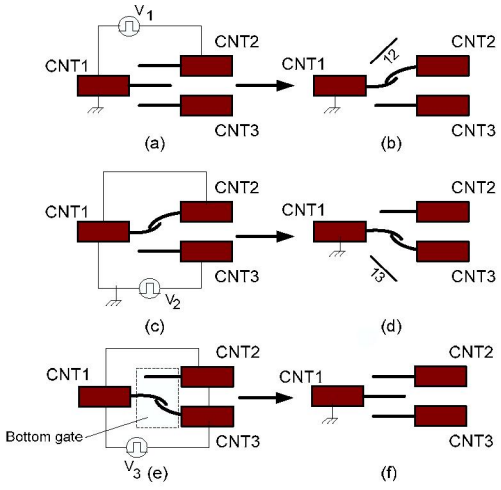


Figure 3. Schematic of CNEMS switching cycles. a) A voltage pulse (V_1) causes CNT1 to be attracted to CNT2. b) the van der Waals force latches CNT1 to CNT2. c) To transition the switch, CNT1 and CNT2 are connected together and a voltage pulse (V_2) is applied between CNT1 and CNT3, d) which unlatches CNT1 from CNT2 and latches CNT1 to CNT3. e) and f) to reset, a bottom gate will be used to apply a voltage pulse to all CNTs .

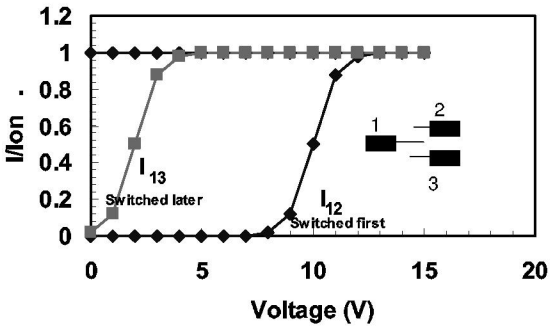


Figure 2. Simulated Switching characteristics of CNEMS (L~50nm, d_1~3.5nm, d_2~3nm, and d_{cnt}~20nm, and δ~10nm). During the programming phase, the threshold voltage is around 10 V. This voltage reduced considerably in subsequent cycles owing to recycling of the stored elastic energy.

The electrostatic potential needed to bend the 50nm-long CNT to achieve defection of δ ~ 10nm is around 10 V (this is calculated by setting $E_{electrostatic} \sim E_{elastic}$). In subsequent switching, however, this voltage will be dropped to around 1 V since a large portion of the elastic energy stored in the CNT will be recovered.

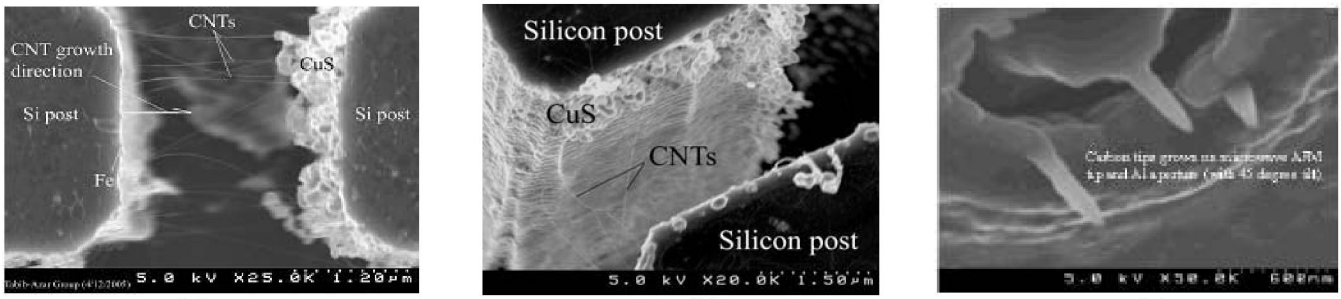
Based on the above considerations, we note that V_{th}~10 V dropping to ~1 volt after the initial cycle as shown in Fig. 2. The main reason for this reduction is that the stored elastic energy causes the center CNT (CNT1 in Fig. 1) to spring back towards the CNT3 when it is released from CNT2. The van der Waals force latching CNT1 and CNT2 is almost entirely balanced out as soon as CNT1 and CNT2 are charged with the same polarity.

To calculate the switching speed we note that the resonant frequency of a CNT (see Fig. 1) is given by: $\omega = \sqrt{\frac{8EI}{mL^3}}$, where "m" is the CNT's mass and the rest of parameters are defined above. For L~50nm, the radial frequency is around 3.16 $x10^{11}$ radian/s corresponding to a frequency of 50 GHz. This yields a transition speed ($v_t \sim \omega L$) of around $1.6x10^4$ m/s that results in transition time ($\tau \sim \delta/v_t$) of around 10^{-12} – 10^{-10} s. The charging time constants may limit the CNEMS speed in the final circuits.

The device isolation resistance in "off" state can be calculated using the tunneling current between two adjacent and non-contacting CNTs as $I \sim I_0 e^{-d_{cnt}/\lambda}$ where λ is approximately the De Broglie wavelength (~10 A) and I_0~0.1 μA (@ 1V). For d_{cnt}~20nm, *I~2x10*$^{-16}$ A that yields an isolation resistance of around $5x10^{15}$ Ω.

The device resistance in the "on" state is given by the sum of contact resistances, the two CNT resistances and the CNT-CNT contact resistance. With good titanium carbide or Pd contacts to the CNTs, the contact resistance can be made small (~1kΩ). The CNT-CNT contact resistance when the two CNTs are touching with an overlap of 30-50nm, is also very small (this will be dictated by tunneling in clean CNTs). The overall resistance will be around 10 kΩ (for ρ_{cnt}~1 kΩ-cm).

The CNTs can be programmed by applying voltage pulses to attract and latch adjacent CNTs to allow for setting the



(a) (b) (c)

Figure 4. a) Carbon nanotubes (CNTs) we have grown using a metal-catalyzed (iron) chemical vapor deposition technique using C_2H_2 between two raised silicon posts. The self-aligned and welded CNTs can be grown into any layer that can withstand the growth temperature of 500-800 °C. b) CNTs grown into a copper layer that was subsequently sulfidized. c) CNTs grown over atomic force microscope tip with co-axial shielding.

current path in the circuit (Fig. 3(b), 3(d)). To "un-stuck" the CNTs, we integrate an electrode under the CNTs so that when a voltage is applied between the bottom electrode and the CNTs, the CNTs are attracted to the bottom electrode that will be covered with a thin oxide layer to prevent current flow but to enable electrostatic actuation. The distance between the CNTs and bottom electrode will be set around 25nm so that the elastic energy of the bent CNTs will be larger than the van der Waals force to prevent latching with the bottom surface. Thus, after the resetting pulse is applied, the CNTs will relax back to their initial pre-programmed state (Fig. 3(f)).

2.3 Defect Tolerance at Device Level

CNEMS's operation critically depends on CNT diameter, length, location, and conductivity. We have developed a metal-catalyzed chemical vapor deposition growth technique that results in the growth of multi-walled and single-walled carbon nanotubes that are self-aligned and self-welded to silicon posts, as shown in Fig. 4. The CNT diameter depends on the diameter of the starting catalyst particles, growth temperature and gas flow rates. These parameters are readily controlled to yield uniform CNT diameter. The post that the CNT grows from (see Fig. 4) is coated with a thin layer of iron (other metal catalysts such as Cu, Ni, etc. that are more compatible with CMOS can also be used). The post that the CNT grows into can be coated with a variety of suitable materials or left as a bare silicon or it can be coated with a sacrificial oxide layer that upon removal will free the CNT tips. To ensure regular CNT lengths, we will use a CNT-growth stop composed of a sacrificial oxide layer. The CNT's growth will be stopped by this oxide layer. Subsequently, the oxide layer will be etched away leaving CNT cantilever beams with nearly identical lengths in place. The CNT location can be specified using nanopores on oxide or similar material or by patterning the catalyst layer. The CNT conductivity depends on the chirality of the graphene layer in single walled CNTs and 2/3 of grown SWCNTs are semiconducting while 1/3 are metallic. By adding another layer to grow double-walled CNTs, majority of DWCNTs become metallic because two layers of different chirality or even the same chirality are shown to produce metallic CNTs.

Thus, the uncertainty in CNT length can be reduced drastically by using sacrificial oxide growth stop layers. The CNT positions can be dictated by using patterned catalyst layer or nanopores/nano-openings, and metallic CNTs can be produced by growing DWCNTs.

3. CIRCUIT IMPLEMENTATION

As described in Section 2, the proposed CNEMS device has fundamentally different principle of operation compared to conventional MOSFET. Thus, logic and memory design with these devices require a major shift in design methodology.

3.1. Logic Behavior of CNEMS

To understand how the proposed switch can be used to realize logic function, let us discuss the behavior of the switch in terms of logical operation. Fig. 5(a) depicts the schematic diagram of the switch, which has three terminals A, B and C. Depending on the voltage differential between the terminals, either A or B (not both) may be connected to terminal C. For a given voltage at A and B, we can consider C as the controlling terminal, which determines configuration of the switch. However, unlike MOSFET, the complementary nature of the CNEMS does not allow a signal path between B and C. From Fig. 5(b), we can observe that by using two-valued logic, CNEMS switch can be taken to one of the four states. Apart from the two states discussed earlier (where terminal C is connected to either A or B), the switch may be completely open (C is not connected to any of A or B) when all

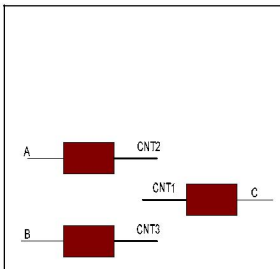
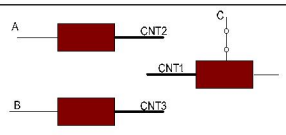
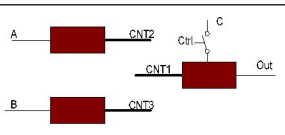


Figure 5. a) Schematic of CNEMS.



A	B	C	State
0	0	0	Open
0	0	1	Indet
0	1	0	B-C
0	1	1	A-C
1	0	0	A-C
1	0	1	B-C
1	1	0	Indet
1	1	1	Open

b) Programming CNEMS.



A	B	C	Out
0	0	0	Open
0	0	1	Illegal
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	Illegal
1	1	1	Open

c) Logical behavior of CNEMS.

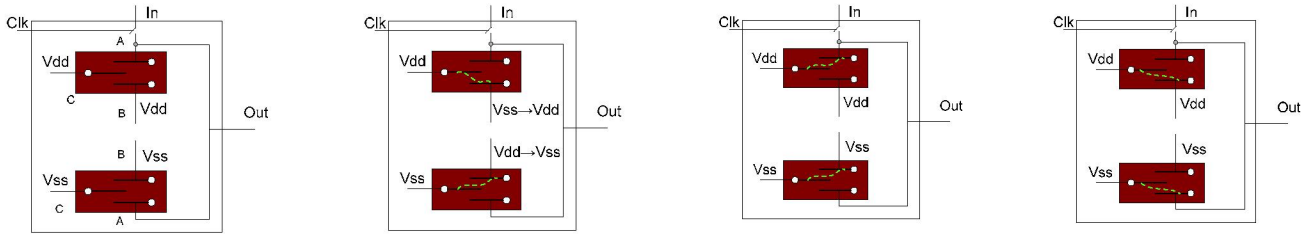


Figure 6. a) An inverting clocked latch design. The complement of the data input at D is latched by the clock. **b) Clocked latch in initial position before writing. With a pulse to the bottom terminals it is "reset" removing history effect.** **c) Latch storing logic 1 in response to a data value 0. Note that it is an inverting latch.** **d) Latch storing logic 0.**

terminals have the same voltage or state of the switch may be indeterminate, when both A and B have the same voltage difference with respect to C. In the later case, position of the switch will eventually depend on the relative strength of the CNTs at A and B, which will be determined by design marginalities like process variations. This state therefore, should be considered as "illegal" with respect to logic design. It can be observed that the switch can be used for pass-transistor like logic implementation. However, it requires two steps to evaluate the logic. In the first step, terminal C can be used to configure the switch by applying appropriate voltage differential. In the second step, terminal C should be disconnected from the controlling input and treated as the output. Fig. 5(c) shows the truth table for the logic operation of the switch with C as controlling input. It can be noted that output terminal has a valid state as long as $A \oplus B = 1$. However, if $A \oplus B = 1$ and terminal C is connected to A, two CNTs connected together (A and C) will be charged with the same polarity and hence terminal C will be attracted towards B, resulting in an unstable state. To avoid this, we can connect two CNEMS devices as in Fig. 6(a), which realizes a stable inverting latch controlled by the clock signal that connects and isolates the input from one of the side terminals. To write a value in the latch, it requires to be configured as in Fig. 6(b), by creating a voltage difference between terminals B and C. Taking the latch to this "reset" state is important to remove history effect and to allow the CNTs to make a transition when the input is connected. Fig. 6(c) and Fig. 6(d) show two valid states of the latch storing logic 1 and 0, respectively.

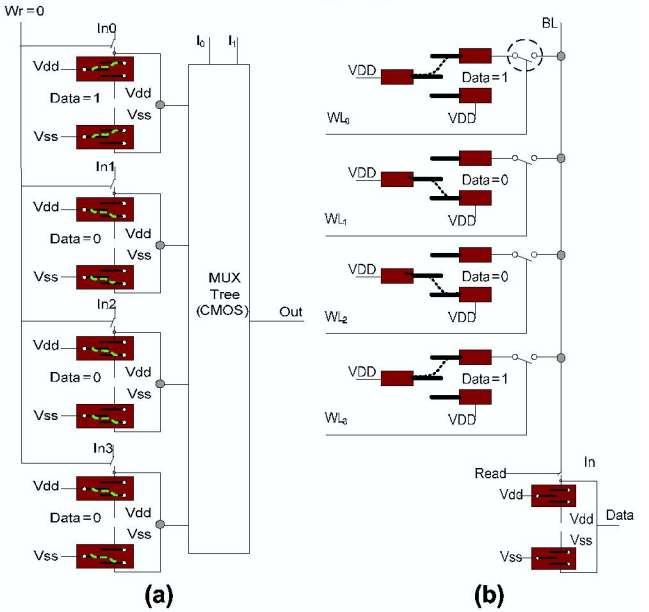


Figure 7. Two possible implementations of a two-input lookup table (LUT) using CNEMS. In (a), decoding is realized with a multiplexer tree implemented with CMOS. A separate decoder and a set of selection switches (circled) are required for the implementation in (b).

3.2 Reconfigurable Logic Fabric

Stable and reconfigurable logic functions can be realized with CNEMS using small memory array organized as lookup table, similar to conventional SRAM-based FPGA [13]. Fig. 7 shows schematic of two possible implementations of a LUT for a 2-input function. Each storage bit is realized by two (Fig. 7(a)) or one (Fig. 7(b)) CNEMS device(s). In Fig. 7(a), the decoding is implemented with a multiplexer tree (implemented with CMOS switches), while in Fig. 7(b) additional decoder and select switches (circled) are required. In the right schematic, depending on the input signals, one of the wordline will be asserted. A common bitline connected to a CNEMS-based latch (Fig. 6) will latch the value. In a multilevel logic implementation using LUT, the schematic in Fig. 7(a) is more efficient in terms of delay, while the one in Fig. 7(b) takes less area. The propagation delay in the left configuration is contributed by scattering-free (ballistic) propagation through the CNTs and signal propagation through the mux-tree. On the other hand, propagation delay on the right configuration is dominated by the transition delay (~1ns) of the sensing CNEMS, which accumulates for multi-level logic.

The CNEMS can also be used, in interesting ways, to realize complex functions with very few basic switches. For

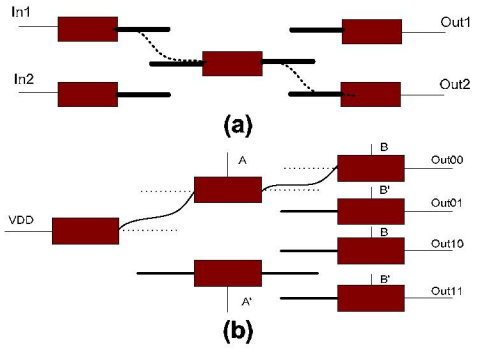


Figure 8. a) Interesting switch matrix using CNEMS; b) Implementation of 2X4 decoder circuit using CNEMS device (configured for A=0, B=0).

Table 1. Comparison of delay and power results between CMOS and CNEMS implementation

Circuit	Delay (sec)		Power (watt)			
	CNEMS	CMOS (70nm, 1V, 100℃)	CNEMS	CMOS (70nm, 1V, 100℃)		
				Dynamic	Leakage	Total
Ripple Carry Adder (4-bit)	6.125e-11	1.392e-10	58.38e-08	6.570e-06	8.972e-06	1.542e-05
Magnitude Comparator (4-bit)	7.877e-11	3.481e-11	18.07e-08	1.859e-06	2.689e-06	4.548e-06
Priority encoder (8:3)	5.252e-11	7.143e-11	23.63e-08	2.470e-06	3.328e-06	5.798e-06
Even Parity (8-bit)	6.127e-11	2.205e-10	29.19e-08	3.701e-06	4.903e-06	8.604e-06

example, Fig. 8(a) shows implementation of a specific crossbar switch matrix where only one output is connected to one input at a time. Fig 8(b) describes a customized implementation of a decoder circuit (2X4), which requires less number of primitive switches and less active power compared to static CMOS implementation. The proposed logic implementations have robust switching operation, low active power for switching states (along with negligible leakage). The reconfiguration can be accomplished at high speed by writing configuration bits to CNEMS switches forcing transition (with ~1GHz transition speed). It is worth noting that since the non-volatile memory cell implemented with CNEMS device is not charge-based, the stored value does not flip due to alpha or neutron particle hit, and hence, completely immune to soft error [14]. The selection switches (connected to the wordline, bit line and data inputs), decoding logic (Fig. 7(b)) and mux-tree (Fig. 7(a)) can be implemented with MOSFET switches for high speed and ease of fabrication.

4. MODELING AND RESULTS

We have used a simple model of CNEMS device schematically shown in Fig. 9. The R12 and R13 are proportional to $1/I_{12}$ and $1/I_{13}$ (Fig. 3). Using the simple model in Fig. 9, we have computed power and performance for a set of circuits implemented with two-input LUT-based functions (as described in Fig. 7(a)). The circuit descriptions were synthesized from Verilog using Synopsys Design Compiler and then mapped to 2-input Boolean functions. In this experiment, we used a hybrid implementation with MOSFET pass transistor (NMOS) for mux-tree and CNEMS switch based storage element. The power and delay for a two-input pre-configured LUTs were contributed by a) two CNTs making a connection and b) a NMOS pass transistor. The bias voltage of the CNEMS device was set to 1V. To compare the effectiveness of CNEMS-based implementation with static CMOS implementation, we computed power and performance for static CMOS realization of the circuits using a 70nm predictive technology model (at 100℃, with a supply voltage of 1V). The simulation results are reported in Table 1. We can observe that the CNEMS based implementation has delay values of the same order as 70nm static CMOS circuits, since the propagation delay in a multi-level CNEMS circuit is contributed by the ballistic transport in the CNTs and signal propagation through the mux-tree. However, in terms of total power, CNEMS implementation consumes orders of magnitude less power compared to CMOS counterparts. Note that the CNEMS in the LUTs do not switch during normal operation and switches only during reconfiguration. The internal energy storage helps to achieve low reconfiguration energy.

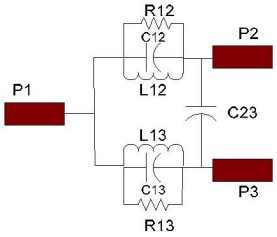


Figure 9. Simple model of the switch that is used in circuit simulations.

5. CONCLUSION

We have proposed a novel Nano Electro-Mechanical switch that exploits unique properties of carbon nanotube. The switch can provide robust low-voltage operation. Two most important features of this device are: a) its internal energy storage and negligible leakage for ultralow-power operation and b) reconfigurability into a non-volatile memory element. The device is amenable to look-up table based reconfigurable logic implementation and can be fabricated with conventional CMOS devices for hybridization. We have developed simple circuit-compatible models of the proposed switch and demonstrated that system development using CNEMS can achieve orders of magnitude power reduction while having equivalent performance compared to a CMOS implementation.

REFERENCES:

1. S. Iijima and T. Ichihashi, "Single-shell carbon nanotubes if 1-Nm diameter," *Nature*, vol. 363, pp. 603–605, 1993.
2. M.S Dresselhaus, G. Dresselhaus, P. C. Eklund, "Science of Fullerenes and Carbon Nanotubes", *Academic Press*, 1996.
3. P. G. Collins, K. Bradley, M. Ishigami, and A. Zettl, "Extreme Oxygen Sensitivity of Electronic Properties of Carbon Nanotubes," *Science*, Vol. 287 (10), pp. 1801, 2000.
4. T. Rueckes et al., "Carbon Nanotubes-Based Nonvolatile Random Access Memory for Molecular Computing," *Science*, Vol. 289, pp. 94, 2000.
5. W. T. Chang et al., "Synthesis of Carbon Nanosphere and Copper-Catalyzed Branched," *APS March Meeting*, 2004.
6. R. P. Feynman, Simulating Physics with Computers, *Int. J. Theory. Physics*, vol. 21, no. 6/7, pp. 467-488, 1982.
7. R. P. Feynman, Feynman Lecture on Computation, Edited by A. J. G. Hey, and R. W. Allen, *Addison-Welsley*, MA, 1996.
8. C. H. Bennett, "Logical Reversibility of Computation", *IBM J. of Res. and Develop.*, vol. 17, pp. 525-532, November, 1973.
9. C. H. Bennett, "The Thermodynamics of Computation - A Review", *Int. J. Theo. Physics*, vol. 21, pp. 905-940, 1982.
10. Massood Tabib-Azar, Run Wang and Yan Xie, "Strain Gauges using Self-Welded Carbon Nanotube Piezoresistors with Very Large Longitudinal Piezoresistivity," *IEEE-NEMS*, 2006.
11. P. G. Collins and Ph. Avouris, "Nanotubes for Electronics," *Scientific American*, December 2000.
12. J. Rabaey, "Digital integrated circuits", *Prentice Hall*, 1996.
13. S. Hauck, "The roles of FPGAs in reprogrammable systems", *Proceedings of the IEEE*, 1998, pp. 615– 638.
14. Richard Phelan, "Solutions for Soft Errors in System on Chip Designs", *D & R Industry Articles*, 2004.