A Novel Wavelet Transform-Based Transient Current Analysis for Fault Detection and Localization

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***Abstract*—Transient current (IDD) testing has been often cited and investigated as an alternative and/or supplement to quiescent current (IDDQ) testing. In this correspondence, we present a novel integrated method for fault detection and localization using wavelet transform-based IDD waveform analysis. The time-frequency resolution property of wavelet transform helps us detect as well as localize faults in digital CMOS circuits. Experiments performed on measured data from a fabricated 8-bit shift register, and simulation data from more complex circuits show promising results for both detection and localization. Wavelet-based detection method shows better sensitivity than spectral and time-domain methods. Effectiveness of the localization method in presence of complex power supply network, measurement noise, and process variation is also addressed.**

***Index Terms*—Fault localization, transient current (IDD), wavelet.**

I. Introduction

A number of research works [1]–[8] have been targeted to establish IDD waveform analysis as an effective technique to detect many of the defects that can occur in ICs, including defects such as resistive opens and weak transistor defects, which may not be detected by conventional IDDQ testing methods. In 1987, Frenzel and Marinos [1] investigated a small time to live (TTL) and described the complete power supply current as a signature of the device under test (DUT). Hasizume *et al.* [2] addressed the issue of analyzing the spectral content of the IDD current under normal and faulty conditions. Beasley *et al.* [3] applied simultaneous pulsing on the power supply rails and analyzed the temporal and/or spectral characteristics of the transient currents. The energy consumption ratio (ECR) for two input transitions was used as a test metric by Vinnakota *et al.* , [4]. Plusquellic *et al.* [5], proposed the concept of Transient Signal Analysis (TSA) with distributed measurement points. De Paul *et al.* [6] used the accumulated charge (computed by numerical integration of a current waveform) for signature comparison. In the method of Sachdev *et al.* [7], one sample per IDD test pattern at a predetermined instance is used as signature. Muhammad *et al.* [8] developed the Discrete Fourier Transform (DFT) based signature comparison to detect faults and an integrator-based approach to extract delay information, which gives an idea about the depth where the fault resides.

While there have been many investigations on fault detection, there is no efficient method for fault localization by analyzing the IDD waveform. In this correspondence, we present an integrated approach for fault detection and localization using the wavelet transform of the IDD signal. The wavelet transform resolves a signal in both time and frequency simultaneously. It gives a better approximation of a transient current waveform than the Fourier transform for a fixed limiting frequency of the current signal, which is determined by the measurement process. Furthermore, the wavelet transform allows us to choose the appropriate basis function for an application, unlike Fourier, where the basis functions are fixed. Hence, for a particular test circuit, we can choose the best suitable basis in terms of approximation error.

In this correspondence, we have demonstrated that the wavelet transform has better sensitivity of fault detection than pure spectral or time-domain analysis of the IDD waveform. Higher sensitivity of fault detection can be useful for detecting faults, which can be masked by other IDD analysis techniques and, thus, can increase fault coverage. We have also utilized the time domain information present in the wavelet coefficients to identify the faulty region. The localization is based on delay measurement technique [8] and can be applicable to both levelized and random logic circuits. Our experimental results are based on measured current data from a 8-bit shift register and transient response obtained from the *HSpice* simulation of an 8-bit Arithmetic Logic Unit (ALU) and an 8×8 Wallace tree multiplier.

The rest of the correspondence is organized as follows. Section II gives an overview of the wavelet transform. Section III explains fault detection and localization using wavelet analysis. Section IV presents experimental results. Section V discusses some important issues about practical application of the method, and Section VI concludes the paper.

II. Overview of Wavelet Transform

Fourier analysis has a serious drawback since it transforms signals in the frequency domain, and information on how the signal is spatially distributed is not readily available. The wavelet transform, on the other hand, decomposes a signal in multiple scales or resolutions and retains both time and frequency domain information in the transform coefficients [9], [10]. In wavelet transform, we take a real/complex valued continuous time function with two main properties: a) It will integrate to zero, and b) it is square integrable. This function is called the mother wavelet or wavelet. Property a) is suggestive of a function that is oscillatory or has wavy appearance, and thus, in contrast to a sinusoidal function, it is a small wave or wavelet. Property b) implies that most of the energy of the wave is confined to a finite interval. The Continuous Wavelet Transform (CWT) of a function $f(t)$ with respect to a mother wavelet $\Psi(t)$ is defined as

$$W(a,b) = \int_{-\infty}^{\infty} f(t)\Psi^*_{a,b}(t)dt \tag{1}$$

$$\text{where} \quad \Psi_{a,b}(t) = \frac{1}{\sqrt{|a|}}\Psi\left(\frac{t-b}{a}\right). \tag{2}$$

Here, a, b are real, and $*$ indicates complex conjugate. $W(a,b)$ is the transform coefficient of $f(t)$ for given a, b. Thus, the wavelet transform is a function of two variables. For a given a, $\Psi_{a,b}(t)$ is a shift of $\Psi_{a,0}(t)$ by an amount b along the time axis. The variable b represents time shift or translation. Since a determines the amount of time-scaling or dilation, it is referred to as scale or dilation variable. If $a > 1$, there is stretching of $\Psi(t)$ along the time axis, whereas if $0 < a < 1$, there is a contraction of $\Psi(t)$. Each wavelet coefficient $W(a,b)$ is the measure of approximation of the input waveform in terms of the translated and dilated versions of the mother wavelet.

III. IDD Analysis Using Wavelet Transform

A. Fault Detection

The fault detection strategy is based on current signature comparison between the DUT and the golden (fault-free) device. Input test stimuli are chosen randomly in our detection process. In a practical test environment, the set of test vectors will often be generated by an Automatic Test Pattern Generation (ATPG) program for IDDQ/IDD testing. Since our objective was to compare the sensitivity of wavelet-based method with other methods, we did not use the ATPG tool. For each stimulus applied to the DUT, we compute the wavelet coefficients of the transient current and compare them with those for the golden device for the same input. The comparison in our case is made by calculating the

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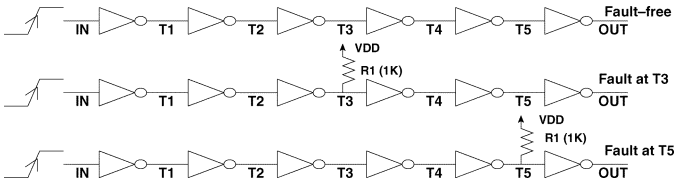

Fig. 1. Inverter chain with bridging fault at T3 and T5.

Root Mean Square Error (RMSE) between the two sets of wavelet coefficients. RMSE is chosen for signature comparison because it is a simple metric with wide popularity. The pass/fail criterion is decided by comparing the value of the RMSE with a preselected test margin.

To compare the effectiveness of our detection scheme with existing methods based on pure spectral and pure time domain contents of the IDD signal, we used a metric referred as normRMS, which is defined in (3). It computes the root mean square of difference between the coefficients for golden circuit response (G_i) and those for the DUT (F_i) as a fraction of the golden circuit coefficient (G_i) for N coefficients. normRMS can be considered to be the measure of detection sensitivity. For the time domain method, we used the charge integration (as discussed in [6]), which uses the accumulated charge under the current waveform for signature comparison.

$$\text{normRMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(\frac{F_i - G_i}{G_i}\right)^2}. \tag{3}$$

B. Fault Localization

In this section, we explain the method to localize fault in a circuit leveraging the time-domain information present in the wavelet components. For a faulty device, we can observe the wavelet coefficients and determine the *delay* at which the response of the faulty circuit deviates significantly from that of the fault-free one. We then use this information to identify a set of suspect cells. There are two advantages of localizing the fault. First, it may be possible to improve the process and yield. Second, we can utilize this information either for fault tolerance or to isolate a small portion of the circuit containing the fault.

Fig. 1 depicts a simple test circuit consisting of a set of inverters in cascade. We use this circuit to explain how we measure *delay* and how it can be used to localize faults. First, we apply input stimuli to the fault-free inverter chain, as shown in Fig. 1, and monitor the IDD waveform using *Hspice*. We then introduce a metal bridge of resistance 1 kΩ between T3 and the supply line and obtain the IDD response. We repeat the same procedure for a similar fault at position T5. Fig. 2 shows the plot of the IDD for these three cases. Fig. 3 shows the wavelet coefficients for the IDD waveform at four different scales. The faulty responses deviate from the fault-free case at some time instant after the transition in the primary input. We call this *delay* between the input transition and the point of deviation in the time axis T_d. This is due to the propagation delay through the cells since the fault is not excited until the effect of an input transition propagates to it. Since the propagation delay to T5 is more than that to T3, the point of deviation for fault at T5 is shifted right in the time axis from the point for fault at T3.

The fault localization algorithm starts by initializing S, which is the set of potentially faulty cells at a particular iteration, with all cells in the DUT. If a fault is detected for an input transition $I_0 \rightarrow I_1$, we compute the *delay* by comparing the fault-free and the faulty responses at multiple scales. Scales corresponding to frequency components below and above some predetermined levels are discarded for *delay* computation. Partition is a method for classifying the cells in the DUT into two nonoverlapping sets—a set of suspects (Sf) and a set of fault-free

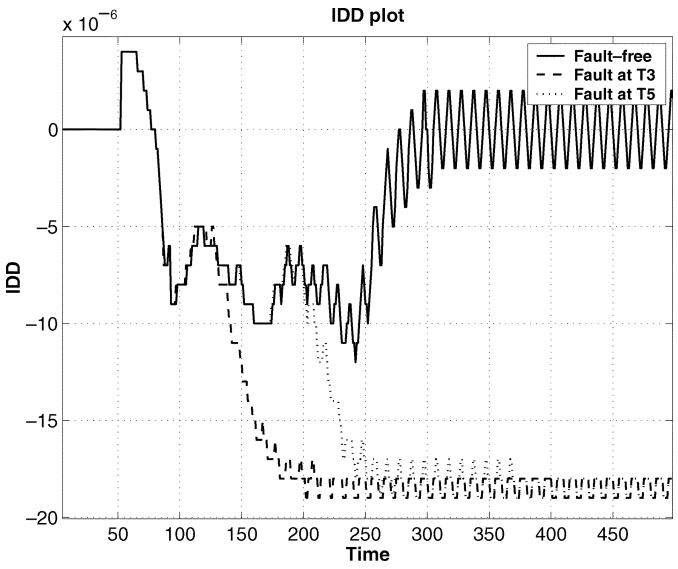

Fig. 2. IDD Waveforms for the inverter chain with and without fault.

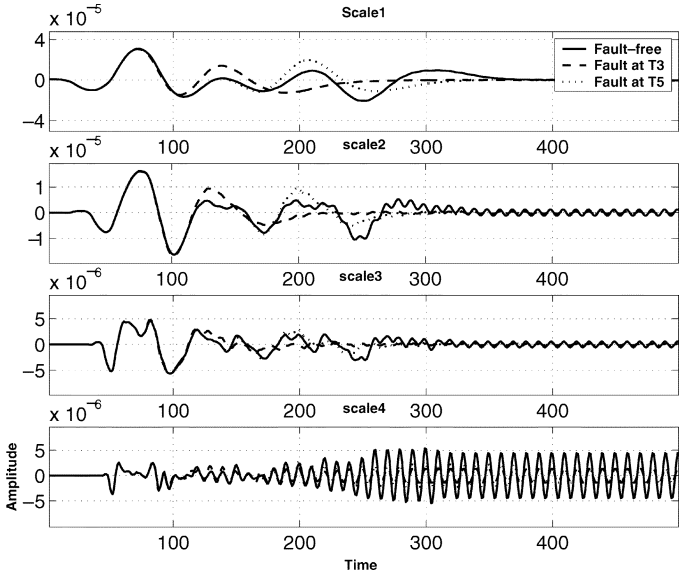

Fig. 3. Plot of Wavelet coefficients at different scales for the IDD waveform in Fig. 2.

cells (Sff)—based on input transition and T_d. At the end of each iteration, the set of suspects (Sf) is intersected with initial set of faulty cells to obtain a more granular faulty region. The partitioning algorithm traverses the cells in topological order starting from the primary input and checks if a particular cell can be considered to be suspect. The process can be iterated multiple times with different input transitions to obtain finer resolution.

Fig. 4 explains the fault localization process. It shows a section of the ALU with a 1 KΩ bridging fault (R1). We applied random input vectors and performed wavelet-based fault detection. If the applied stimulus activates the fault, the delay in activation of abnormal current would manifest itself in the current waveform. This delay is computed using wavelet coefficients. Fig. 4 shows faulty regions identified with two different input vectors. First, we identify a region x1 for an input vector. For the next input vector, we get region x2 as the potential faulty region. We take the intersection of the two regions to localize the fault more precisely.

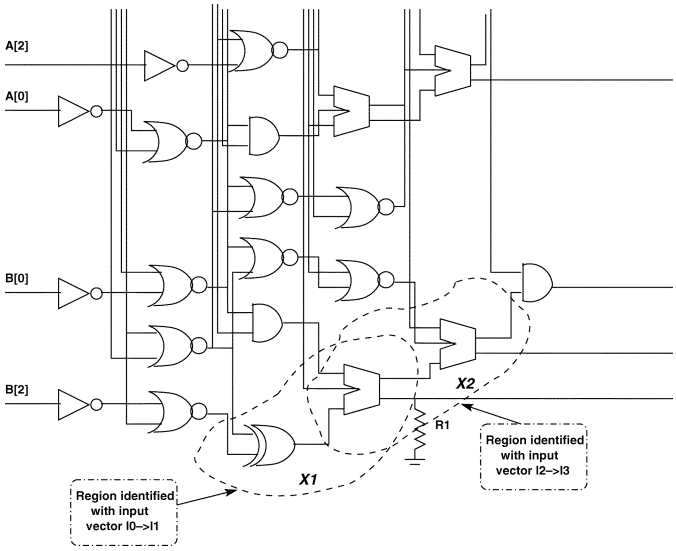

Fig. 4. Localization process identifies region x1 and x2 for different input stimuli.

It is worth noting that for initial iterations of partitions, the suspect cells may come from different parts of the circuit, but successive iterations with different input transitions tend to eliminate the suspects, which are remote to the faulty candidate. Thus, the localization process can determine a faulty region consisting of a set of adjacent cells.

Wavelet coefficients give us a more efficient way to calculate T_d than using simple integration [8] or a point-by-point comparison of the IDD signal. The wavelet transform can resolve a signal in time axis at different scales or frequencies. Hence, we can compute T_d for multiple frequency components simultaneously using wavelet decomposition. This helps us get rid of the dc component in the IDD automatically. We can also avoid the *aliasing* effect, which may be present in the integration-based method.

IV. Experimental Results

The detection and localization algorithm was implemented in *C* programming language. We used *Matlab* wavelet toolbox [11] to perform wavelet (CWT) and Fourier decomposition (FFT) of the IDD signal. The mother wavelet used in wavelet transform was *db2* [9]. We have chosen "db2" as our mother wavelet, because it is a popular basis wavelet and is compactly supported and orthogonal [10]. It can give good mapping of the input waveform for our applications. The algorithm was tested on the measured data from the fabricated test chip for an 8-bit shift register and on simulation data from more complex circuits. Different scales of the mother wavelet correspond to different spectral content of the basis. Hence, we choose a limiting frequency (400 MHz in our case) and use both Fourier and wavelet components up to that frequency, starting from the dc value. We have used four different scales for wavelet decomposition, which correspond to 16 spectral components in the DFT for a limiting frequency of 400 MHz. The scales in the wavelet transform were dyadic (power of 2) starting from 8 to 64. The frequency content of the mother wavelet for different scales is determined by taking the 20-dB point in the spectrum as the cutoff. The lowest value of scale, i.e., 8, corresponds to the highest frequency and is selected on the basis of the upper margin (400 MHz), whereas the highest value of scale, i.e., 64, is selected because it has a very narrow spectrum around dc. Any higher value of scale did not result in a significant change in mapping error. In the DFT-based method, we consider both magnitude and angle (phase) components of a coefficient for computing normRMS. The absolute difference between corresponding components for faulty and nonfaulty cases is then normalized with respect to the corresponding component in the nonfaulty case. We use (3) to compute the RMS of these normalized values. For normRMS of charge, we take the absolute difference in the area under the IDD curve (obtained from numerical integration) normalized to the area for the nonfaulty case.

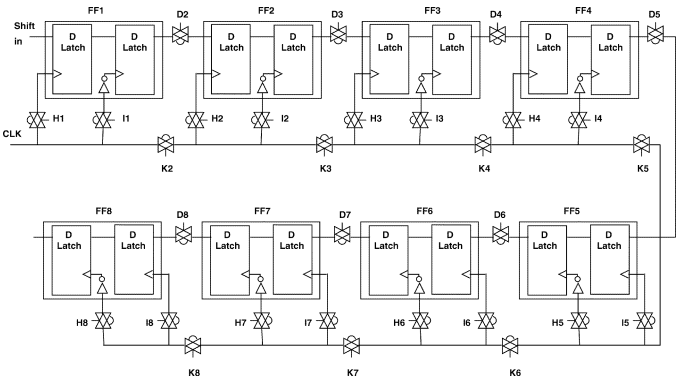

Fig. 5. Eight-bit shift register used to measure the transient current.

TABLE I
Comparison of Sensitivity of Wavelet-Based Detection With DFT and Charge Integration Techniques

Fault	$normRMS$ (Wavelet)	$normRMS$ (DFT)	$normRMS$ (Charge)
K2	5.563	1.184	0.973
K3	4.519	1.040	0.948
K4	5.979	0.806	0.922
K5	4.812	0.889	0.872
K6	5.246	0.948	0.813
K7	6.321	1.564	0.698
K8	5.212	1.462	0.544

A. Results for a Fabricated 8-Bit Shift Register

The experiments used an 8-bit shift register in which several mask defects were designed. Transmission gates were connected to selected nodes of the circuit to emulate the presence of open defects. When a transmission gate is off, the corresponding open defect is activated. Fig. 5 is the schematic of the shift register with the transmission gates labeled for each defect. The circuit was designed with ES2 n-well dual metal 1.0-μ technology. Current was measured by sensing the voltage drop at a very low inductive MP930 Caddok 300-Ω resistor with a Tektronix P6247 1-GHz bandwidth differential probe. To test the wavelet-based detection and localization method, we worked with open defects (at K2, . . ., K8) preventing clock propagation from the defect site to the register. Details about the input vectors selected to activate the faults and the measurement process can be found in [6].

Table I presents comparative results for the detection sensitivity of the wavelet, DFT, and charge integration-based method. The fault K_i implies that the transmission gate between the clock line and the ith register (Fig. 5) is open. It can be observed that the sensitivity for the wavelet-based method is significantly higher than either the DFT or charge integration methods. This difference is plotted in Fig. 6. The superior sensitivity of the wavelet can be attributed to its decomposition of the IDD signal in both the time and frequency axis and better approximation of the signal at a particular frequency band.

Table II presents the localization results for the open defects in Table I. The delay T_d to each node K_i is computed from the *Hspice* simulation of the extracted layout, which is then compared with the delay obtained from comparing the wavelet coefficients of the

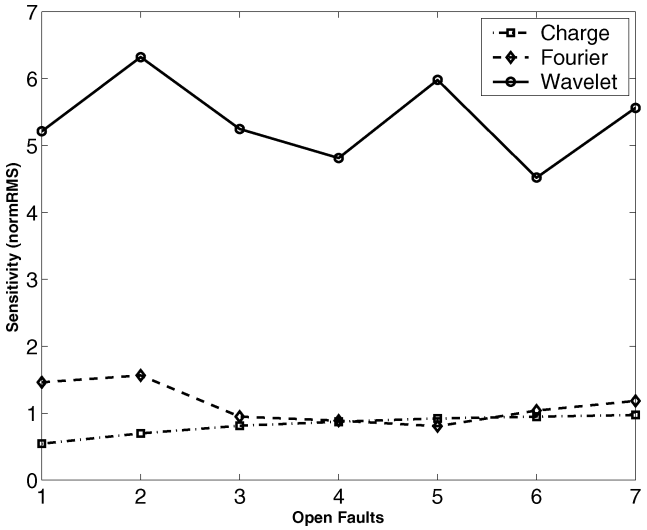

Fig. 6. Comparison of fault detection sensitivity for the fabricated chip.

TABLE II
LOCALIZATION RESULTS (IN TERMS OF DELAY) FROM THE TEST CHIP

Fault	Delay from measured data (ns)	Delay from simulation (ns)	% Variation
K2	2.50	2.20	13.6
K3	7.00	7.60	7.8
K4	11.50	12.00	4.1
K5	14.20	15.53	8.6
K6	16.25	17.83	8.9
K7	19.50	19.88	1.9
K8	21.75	20.00	8.8

TABLE III
COMPARISON OF DETECTION SENSITIVITY FOR ALU AND WALLACE TREE MULTIPLIER CIRCUIT

Design	Fault	$normRMS$ (Wavelet)	$normRMS$ (DFT)	$normRMS$ (Charge)
8-bit ALU	Bridge (Vss)	35.771	0.071	0.313
	Bridge (Vdd)	23.954	0.063	0.246
	open	15.464	0.026	0.150
	Bridge (Vss)	251.005	0.816	0.685
WTM (8x8)	Bridge (Vss)	7.635	0.268	0.063
	Bridge (Vdd)	3.493	0.157	0.238
	Open	88.779	1.285	0.196
	Bridge (Vdd)	27.016	1.678	0.218

TABLE IV
FAULT DETECTION AND LOCALIZATION RESULT FOR AN 8-BIT ALU

Fault	Detected/ Located	# vectors	Cells in faulty region	% of total cells
Metal bridge (with VDD)	Yes/ Yes	13	71	7.00
Metal bridge (with GND)	Yes/ Yes	7	91	8.88
Gate oxide short	Yes/ Yes	16	52	5.13
Open	Yes/ Yes	3	72	7.10
Metal bridge (with GND)	Yes/ Yes	4	62	6.11

measured current and that obtained from simulation. The localization of the fault depends on how accurately we can measure the delay. The delay obtained from the measured data varies below 8% on average, which is good enough to identify the fault location, i.e., which transmission gate is open.

B. Simulation Results for More Complex Circuits

Wavelet-based detection and localization were tested on simulation data from more complex circuits. Two test circuits used are an 8×8 Wallace tree multiplier with about 800 cells and an 8-bit integer ALU with about 1000 cells, both implemented with the LEDA standard cell library. We introduced different types of faults and simulated the circuit with *Hspice* for a 0.25-μ TSMC technology library. Random input stimuli were applied to detect and localize faults. We use 10-Ω resistance to model a bridge and 1-MΩ for an open.

Table III demonstrates the sensitivity of wavelet-based detection compared to the DFT and charge-based techniques. Resistive shorts and opens are used for comparison. For all the cases, the wavelet has a much higher sensitivity than the DFT and charge integration techniques, proving its effectiveness for larger circuits. We have also studied the impact of varying the resistance for bridging faults. The detection sensitivity decreases with an increase in the value of bridging resistances for all three cases. A deviation in the supply current waveform becomes less and less obvious with increasing resistance. Since the wavelet transform models any deviation better than the others, however, it maintains the advantage of having the highest sensitivity for different bridging resistances.

Table IV shows our experimental results for different types of faults injected in the test circuit at random locations. We successfully detected and localized faults in all cases. How narrowly we can identify the faulty region largely depends on the number of input stimulus applied. We terminated our localization process if either we were able to localize the fault in 10% of the total cells or if we had run 20 iterations of *Partition*. This was done to limit the slow *Hspice* run. Column 3 lists the number of random test vectors used (tests that detect the fault). Column 4 shows the number of cells in the identified region, which measures how accurately we can localize the faults. Column 5 lists the number of cells in the faulty region as a percentage of total cells in the circuit.

V. FACTORS AFFECTING LOCALIZATION

A. Effect of Power Supply Network

Our experiments assume that the circuit consists of only one module that is directly connected to the power supply pin. More realistically, the power supply network can be modeled as a mesh-like grid with different modules connected at single or multiple points on the grid. It can be observed that our localization method can be effective if the occurrence of a fault in a module does not significantly affect the current waveform in others. Localization depends on determining the point of deviation in the current waveform, which can be wrongly detected if current drawn by nonfaulty modules change due to a fault in an adjacent module. We simulated a power grid,, which is described as an RLC mesh with three different modules—an adder, a multiplexer and a comparator—connected to different points on the grid. The mesh structure and the RLC model of the power supply network are taken from [12]. We have observed that for several faults injected in the modules, we can determine the *delay* correctly. Both detection and localization work for a mesh-like power supply network.

B. Mother Wavelet Selection

The choice of mother wavelet is another issue that may affect computation of the T_d and, thus, localization. One of the advantages of wavelet transform is that it is adaptive, i.e., we can select a mother wavelet that can best approximate the input waveform. We experimented with a number of mother wavelets, e.g., *db2*, *morlet, Mexican hat, Haar*, etc. [9], [10] and observed how T_d differs for different wavelets for a particular bridging fault in the ALU. For a particular test circuit, we can empirically determine the best basis wavelet, which can give the best average localization resolution for a number of vectors and a set of different faults. The option of choosing an appropriate basis function involves some extra work, but it needs to be done only once for each test circuit. Among the mother wavelets we have examined, orthogonal wavelets with compact support (e.g., *db2*) usually give very good mean square error since they closely match the supply current waveform.

C. Effect of Sampling Frequency and Measurement Noise

The sampling rate at which the IDD waveform should be monitored is important because it affects the measurement noise and applicability of the method in real time. Ideally, we need to sample the IDD waveform at above the Nyquist rate (i.e., twice the maximum frequency) to keep all the frequency components in the sampled data. However, to detect a fault, it is observed that we do not need high sampling frequency. The hardware used to measure the IDD waveform has some fixed resolution and can typically sample current waveforms in the several Megahertz range. Furthermore, the current waveform measured off-chip loses some high-frequency components due to the presence of decoupling capacitance and input pin capacitance.

Although we have used a sampling frequency of 50 ps in our measurements, our fault detection and localization methods use frequency content of the current waveform below a limiting frequency of 400 MHz. Both detection and localization work reasonably well for the frequency range we have considered. As the testing frequency diminishes, the wavelet transform will still have a better approximation and sensitivity than the DFT, but the absolute value of detection sensitivity and resolution of the faulty region will diminish.

D. Process Variation

Process variation has significant impact on IDD testing, and several techniques [4] have been proposed to deal with process variation. Therefore, it is necessary to take into account the impact of process variation in determining test margin for fault detection. Process variation also affects the propagation delay along a path, primarily because individual cell delays vary with process parameter changes. Hence, the localization process also seems to be affected.

To investigate the effects of process fluctuation on wavelet-based testing, we used a simple model for process variation by changing transistor threshold (Vth) [13]. We performed both detection and localization with uniform Vth variation by $+/-$ 5-10%. We have observed that if we compute test margins (the pass/fail limit) based on 10% Vth variation, we can still detect all the faults effectively. Table V lists our experimental results for localization with variations in Vth for a particular bridging fault in the ALU. The impact of process variation on the localization, as shown in Table V, is in terms of the resolution of the faulty region. While the granularity of the identified region decreases due to inaccuracy in the *delay* estimation, it can still localize the fault.

TABLE V
EFFECT OF PROCESS VARIATION ON LOCALIZATION

Vth change		# vectors	Cells in faulty region
NMOS	PMOS		
0%	0%	7	90
5%	5%	7	92
5%	-5%	7	92
-5%	5%	7	95
10%	10%	10	101

VI. CONCLUSIONS

We have demonstrated that multiresolution analysis of the IDD waveform using the wavelet transform can be effective for fault detection and localization in digital circuits. Generation of the optimal set of input stimuli for fault detection and localization is necessary to make the testing process more efficient. The execution time of the localization process and the granularity with which we can identify the faulty region substantially depends on the set of input vectors chosen.

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