Dynamic Supply Current Testing of Analog Circuits Using Wavelet Transform

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Abstract

Dynamic supply current (IDD) analysis has emerged as an effective way for defect oriented testing of analog circuits. In this paper, we propose using wavelet decomposition of IDD for fault detection in analog circuits. Wavelet transform has the property of resolving events in both time and frequency domain simultaneously unlike Fourier expansion which localizes a signal in terms of frequency only. Wavelet transform also has better sub-banding property and it can be easily adapted to current waveforms from different circuits. These make wavelet a more suitable candidate for fault detection in analog circuits than pure time-domain or pure frequency-domain methods. We have shown that for equivalent number of spectral components, sensitivity of wavelet based fault detection is much higher than Fourier or time-domain analysis for both catastrophic and parametric faults. Simulation results on benchmark circuits show that wavelet based method is on average 25 times more sensitive than DFT (Discrete Fourier Transform) for parametric faults and can be considered as a promising alternative for analog fault detection amidst measurement hardware noise and process variation.

I. Introduction

In recent years we have seen rapid evolution in analog and mixed-signal integrated circuits(ICs) in mobile and multimedia devices. This represents a relevant part of the market in production volume and applications. The integration of this type of circuits improves performance, cost and flexibility but complicates both the design and testing process. Analog and mixed-signal circuits have emerged more difficult to test than digital CMOS circuits and testing of the analog parts contribute significantly to the total manufacturing cost.

One important reason for the difficulty of analog testing is the effect of parametric variations which can cause the behavior of the fault-free device to deviate significantly from nominal values, masking the effect of the fault [1]. Cost of test increases in proportion to the precision required for testing with tolerance for parametric variations [2]. An efficient test method needs to be sensitive enough to precisely identify the deviations beyond the tolerance limit.

The slow and expensive nature of specification testing has motivated research into fault-based or structural test for analog circuits. Voltage measurement based techniques cannot access the internal nodes and has poor fault coverage for analog circuits. IDDQ testing in analog circuits have been explored because of its high fault coverage but it has problems like very high steady state currents in many analog circuits [3]. On the other hand, measurement of dynamic power supply currents has been found very useful for testing analog or mixed-signal ICs because of its potential to detect large class of manufacturing defects [4] [5] [6]. The current passing through the VDD or GND pin is measured under application of an input stimuli and the waveform is used to detect fault. While the waveform contains significant information about the circuit performance, appropriate analysis is required to extract specific knowledge about the signal. Existing analysis methods based on statistical or spectral properties of current waveform are effective for catastrophic faults but does not work well for parametric faults, which are more difficult to detect.

In this paper, we present a wavelet based dynamic current analysis method for fault detection in analog circuit. We show that wavelet decomposition has better sensitivity to detect parametric faults than techniques which use spectral or time domain information separately. Wavelet transform of a signal is a two-dimensional decomposition technique which analyzes the signal in multiple resolutions. Coefficients corresponding to each resolution localize events in time domain. Hence, wavelet transform coefficients of a signal contains both time and frequency information making it more sensitive for fault detection. In our work, we have used a simple metric for comparing the sensitivity of the wavelet method with DFT based method and a time domain method. Simulation results on two benchmark circuits demonstrate the superiority of wavelet method for parametric faults.

The rest of the paper is organized as follows. Section II describes previous work on supply current testing of analog circuits. Section III presents basic ideas about wavelet transform. Section IV deals with fault detection using wavelet transform of the IDD signal. In section V we present the simulation results. In Section VI, we consider some important issues for analog fault detection using wavelet. Section VII concludes the paper.

II. Previous Work on IDD testing for Analog circuits

Some of the initial work on IDD testing was done by Frenzel and Marinos [7] in 1987. They investigated a small TTL and described the complete power supply cu

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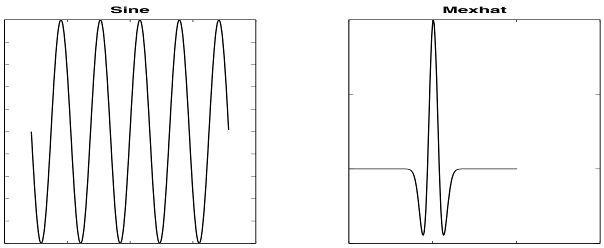

Fig. 1. Basis functions for Fourier and wavelet transforms

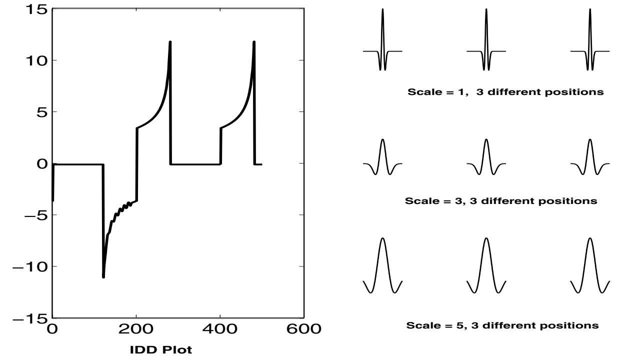

Fig. 2. IDD waveform from a digital to analog converter with parametric fault (left) and *mother wavelet* at different *scale*s and positions used in wavelet transform

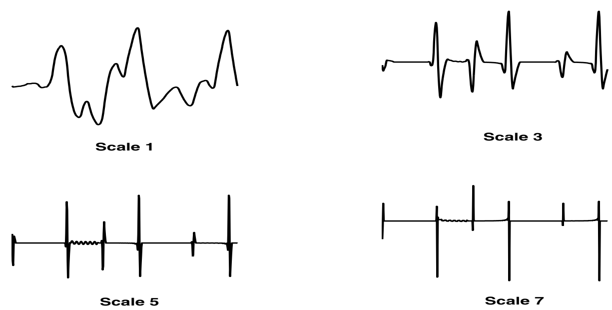

Fig. 3. Wavelet coefficients at different *scale*s obtained from current waveform in figure 2

a signature of the Device Under Test (DUT). Camplin et al. [6] explored the suitability of supply current monitoring as a unified technique for the testing of analog and digital portions of Mixed ASICs. They used the absolute value of the supply current level for different set of input stimuli as signature.

Gielen et al. [5] presented a new method for testing both DC and AC faults in analog circuits. Time domain testing followed by DFT based spectral analysis is applied to detect faults. Beasley et al. [8] investigated an IDD pulse response testing by pulsing the power rails and analyzing temporal and/or spectral characteristics of the transient current. Graeb [4] et al. use process specific (parameter statistics) and circuit specific (performance specification) fault model. They used DFT based signature comparison to detect faults.

Vinnakota [2] suggested a method to detect fault in CMOS circuits by monitoring the dynamic power dissipation. The change in power dissipation caused by a fault can be controlled by changing input patterns. This scheme can be used to detect faults which do not affect static power dissipation. But it needs each test vector pairs to be applied multiple times at full speed to produce a measurable difference in power dissipation and thus can be very slow.

Spinks [11] dealt with the issue of process parameter variation and the choice of correct stimulus for optimum fault coverage in analog circuits. They chose the best test stimuli using sensitivity analysis and then produced the test margin by fault simulation considering process variation. It is directed specifically to detect *hard* faults using RMS (Root Mean Square) supply current monitoring. Somayajula [10] et al. used fault dictionary based approach to detect fault but applied ramp input to obtain better fault coverage. Y. Kilic and M. Zwolinski [1] used both the RMS value of the AC supply current as well as the DC current level to detect faults in analog circuits. They varied the supply voltage at fixed steps to improve fault coverage.

While supply current analysis has been well-studied for fault detection in analog circuits, an efficient current analysis technique which works well for parametric faults in presence of measurement noise was not established. In this paper, we have investigated the potential of wavelet transform as a supply current analysis technique with significantly greater detectability of faults.

III. An Overview of Wavelet Transform

Wavelet transform is a mathematical operation that decomposes input signal simultaneously into time and frequency components [13][14]. Fourier analysis has a serious drawback since it transforms signal in frequency domain losing all information on how the signal is spatially distributed. Hence, it is impossible to localize an event in time scale looking into the Fourier coefficients of a signal. Wavelet decomposition of a signal, on the other hand, can resolve events in both time and frequency domain, which turns out to be very useful in fault detection. In wavelet transform we take a real/complex valued continuous time function with two properties - a) it will integrate to zero, b) it is square integrable. This function is called the *mother wavelet* or wavelet. (This has to satisfy another property called *admissibility*, to perform the inverse transform). Property (a) is suggestive of a function which is oscillatory or has wavy appearance and thus in contrast to a sinusoidal function, it is a small wave or wavelet (figure 1). Property (b) implies that most of the energy of the wave is confined to a finite interval. The CWT or the Continuous Wavelet Transform of a function $f(t)$ with respect to a wavelet $\Psi(t)$ is defined as:

$$W(a,b) = \int_{-\infty}^{\infty} f(t)\Psi^*_{a,b}(t)dt \qquad (1)$$

$$\text{where } \Psi_{a,b}(t) = \frac{1}{\sqrt{|a|}}\Psi\left(\frac{t-b}{a}\right) \qquad (2)$$

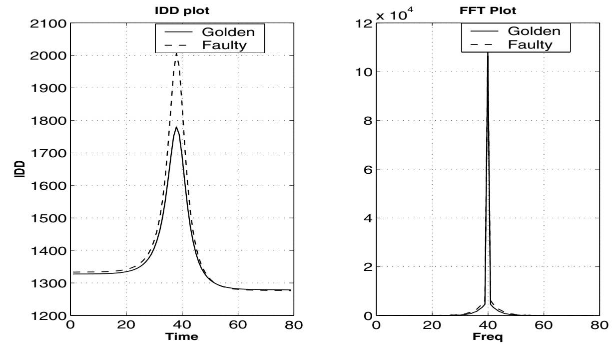

Fig. 4. IDD and DFT plot for a faulty response (parametric fault) of an analog filter

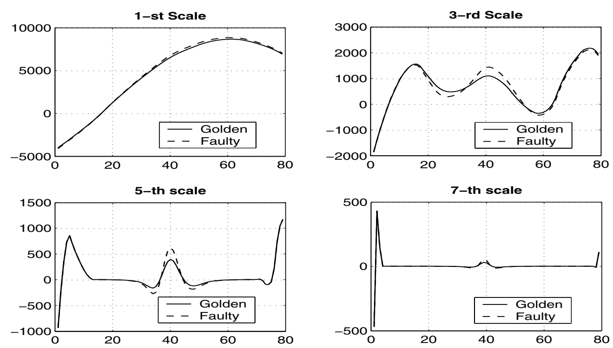

Fig. 5. Corresponding wavelet components at 4 different scales

Here a,b are real and $*$ indicates complex conjugate. $W(a, b)$ is the transform coefficient of $f(t)$ for given a, b. Thus the wavelet transform is a function of two variables. For a given a, $\Psi_{a,b}(t)$ is a shift of $\Psi_{a,0}(t)$ by an amount b along time axis. The variable b represents time shift or translation. Since a determines the amount of time-scaling or dilation, it is referred to as *scale* or dilation variable. If $a > 1$, there is stretching of $\Psi(t)$ along the time axis whereas if $0 < a < 1$ there is a contraction of $\Psi(t)$ (figure 2). Each wavelet coefficient $W(a, b)$ is the measure of approximation of the input waveform in terms of the translated and dilated versions of the *mother wavelet*. Figure 1 compares the basis signals of DFT and wavelet transform. The *mother wavelet* shown in figure 1 is called *mexican hat* wavelet. Figure 2 shows the translated and dilated *mother wavelet* used to approximate an IDD waveform of an analog circuit. Figure 3 shows the wavelet components of the IDD signal in figure 2 at four different *scales*. It can be noted that components have rapidly diminishing magnitudes at higher frequencies (higher *scale*s).

IV. **Fault Detection Using Wavelet Transform**

Figure 4 plots dynamic supply current responses for a fault-free and faulty (parametric fault) analog filter with their corresponding DFTs. Figure 5 plots the wavelet components of these responses at different *scale*s. It can be observed that wavelet components capture more variation in their value than DFT and they represent the variation in the IDD waveform better than DFT. The proposed wavelet based fault detection process is similar to existing Root Mean Square(RMS) error measurement technique that uses the dynamic current of the circuit [9]. Dynamic supply current of an analog circuit is observed in response to a transient input stimuli. The sampling rate should depend on the specific precision required and frequency content of the response. Current waveform is then subjected to wavelet transform to generate a two dimensional set of coefficients. In case of wavelet decomposition, we need to choose an appropriate basis function (*mother wavelet*) unlike DFT, which has a fixed basis.

The two dimensional set of wavelet coefficients obtained from a test circuit (DUT) for a particular input stimuli, is then compared with those from a golden circuit for the same stimuli. We compute the RMS error between the coefficients for comparing the response of the DUT with golden circuit. An RMS error which is more than a predetermined test margin indicates a faulty DUT. The precision of the testing process depends on the quality of the test margin. Manufacturing process parameter variations and measurement hardware noise need to be taken into account in identifying test margin. In addition, the success of the test largely depends on the choice of input stimulus which plays important role in determining fault coverage [11].

In this research, our goal is to show wavelet transform as a more efficient dynamic current waveform analysis than DFT and other statistical methods [1] [5] for detecting faults in analog circuits. We have chosen a simple RMS error metric for comparing the sensitivity of the wavelet based testing with DFT or time-domain method. The reason for choosing RMS metric over other is its simplicity and wide popularity. In the following equations G_i's are the coefficients for golden circuit response and F_i's are those for DUT response. Equation 3 represents the RMS value of difference. The normalized RMS, as in equation 4 can be considered a direct measure of the sensitivity of the transforms. In equation 4, we use the fault free components (G_i) for normalization. It computes the root mean square value of the difference as a fraction of the corresponding golden circuit coefficient(G_i). In addition to DFT method, we also use a pure time domain approach based on charge computation (area under supply current curve) to compare the wavelet method.

$$RMS = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(F_i - G_i)^2} \quad (3)$$

$$normRMS = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(\frac{F_i - G_i}{G_i}\right)^2} \quad (4)$$

V. **Simulation Results**

To compare the effectiveness of wavelet transform based fault detection with existing analysis techniques, we applied the methods on two benchmark circuits and observed their performance using sensitivity metric mentioned earlier. One of the circuits is a leapfrog filter (figure

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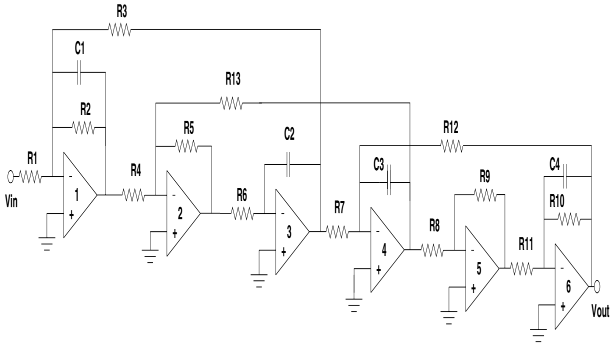

Fig. 6. Analog benchmark circuit : leapfrog filter *(ITC'97)*

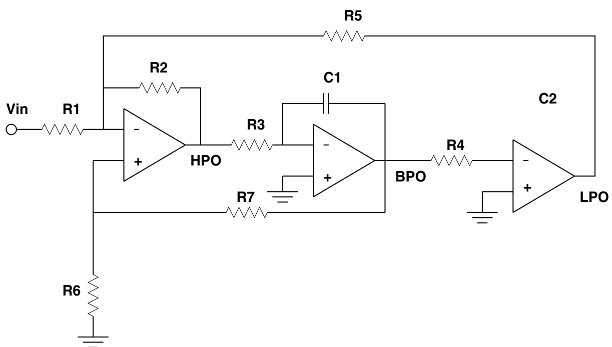

Fig. 7. Analog benchmark circuit : continuous-time state-variable filter *(ITC'97)*

the other is a continuous-time state-variable filter (figure 7). Both are taken from the ITC'97 set of benchmarks. We performed simulations on the *Hspice* netlist of the circuits with AC input stimuli for both the circuits. The *mother wavelet* chosen was *db2* [13]. We used Matlab software for computing the DFT and wavelet coefficients. To model catastrophic faults we used a bridging resistance of 10 Ω for shorts. Opens were modeled using a 100M Ω resistance. Parametric faults were modeled either by +/- 6 σ variation in circuit component or by varying the transistor threshold voltage (Vth). We used the same number of frequency components for both wavelet and DFT methods. Coefficients with value less than 1 were not considered to compute the normalized error.

Table I shows the result of comparison for parametric faults in both the circuits. 'LF' stands for circuit leapfrog filter and 'CTSV' for continuous-time state-variable filter. Column 2 specifies the kind of parametric fault introduced in the circuit. Column 3 and 4 are the RMS error for wavelet and DFT method respectively. Column 5 (ERRQ) is the error calculated as difference in area under current waveform while the column 6, 7 and 8 represent the normalized error value for all three cases. It can be observed that the wavelet based method has significantly better sensitivity than the other two methods. The average sensitivity for wavelet is about 25 times of DFT and about 80 times of the charge based method (NormQ) for the 10 parametric faults considered in table I.

The test margin for the catastrophic faults should fall outside the test margin required to detect the parametric faults. To verify that it is true for wavelet based testing, we experimented with a set of catastrophic faults in the leapfrog filter and computed the sensitivity. Table II shows that catastrophic faults can be detected using the test margin for parametric faults and wavelet based method has the better sensitivity measure also for the catastrophic faults.

For table I and table II the number of frequency components used is 8 starting from the lowest frequency component for both wavelet and DFT methods. It is observed that the DFT coefficients converge to zero at a very slow rate and we can get equivalent sensitivity in DFT method only if we consider large number of frequency components. Table III presents the number of frequency components for DFT, that is required to have normalized RMS equivalent to that in wavelet using 4 frequency components.

Figure 8 plots the fault coverage of two methods to compare their effectiveness to detect fault for a fixed normalized error. We considered a total of 23 parametric and 5 catastrophic faults in two test circuits. The plot shows that for a Normalized RMS error of 0.25 we can detect 1.6 times more faults using wavelet while it is 5.8 times for an error bound of 5. The plot in figure 9 compares the distribution of normalized RMS for two cases. For this plot we considered 10 parametric faults as in table I. It can be noted that the error distribution for wavelet has more deviations across faults than DFT.

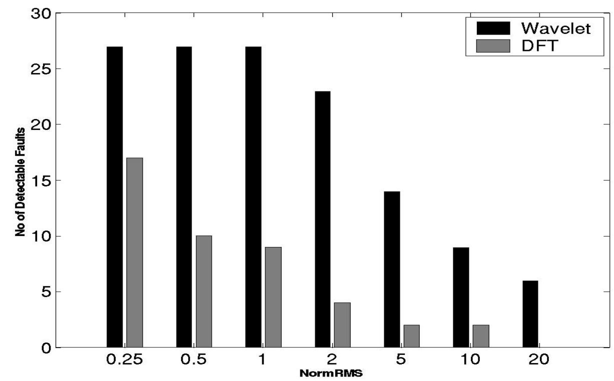

Fig. 8. Comparison of fault coverage for wavelet and DFT method.

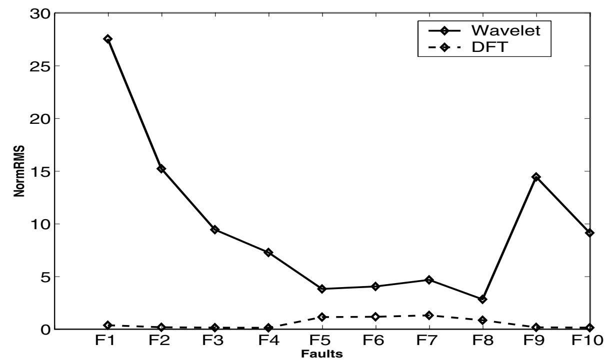

Fig. 9. Distribution of Normalized RMS for 10 different faults.

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TABLE I

Comparison of sensitivity for parametric faults

Design	Fault	RMS(W av)	RMS(DFT)	ERRQ	$NormRMS$(W av)	$NormRMS$(DFT)	NormQ
LF	C4, +6s	525962.0	627369.9	575.2	1.86	0.24	0.11
	C2, -6s	1179645.0	969349.8	869.3	7.41	0.45	0.17
	R1, -6s	3809144.3	6193127.5	2456.5	3.68	0.61	0.47
	R2, -6s	2190771.0	3554285.6	1845.3	2.74	0.51	0.35
	Vt, +10%	248464.0	402469.6	626.5	0.24	0.04	0.12
CTSV	C1, -6s	2094.3	1422.6	33.1	27.57	0.40	0.10
	C1, +6s	1465.9	976.9	27.1	15.26	0.23	0.08
	C2, +6s	836.9	607.4	20.3	7.30	0.17	0.06
	R7, +6s	2417.0	2937.7	40.5	4.10	1.22	0.12
	R5, +6s	9954.8	11362.3	100.1	32.10	1.67	0.30

TABLE II

Comparison of sensitivity for catastrophic faults

Fault	RMS(W av)	RMS(DFT)	ERRQ	NormRMS(W av)	NormRMS(DFT)	NormQ
R8, VCC bridge	59724930.8	83412522.5	8936.2	142.61	10.21	1.69
C2 shorted	16354037.4	26511764.3	5075.5	15.73	2.72	0.96
Drn/Src short, Opamp4, M3	14492540.8	21761478.2	4571.2	51.36	2.04	0.87
R5 Open	27378158.7	28496386.6	4910.6	1228.67	11.74	0.93
Drn/Gate short, opamp5, M7	7173998.5	10345002.0	3135.3	22.44	1.41	0.59

VI. Test Design Issues

A. Choice of *mother wavelet*

Selection of basis for wavelet analysis (*mother wavelet*) has impact on the sensitivity of fault detection. This is observed in table IV. In this table, we list the RMS and normalized error value for two different faults using different *mother wavelet*s. For the test circuit (leapfrog filter) and the faults considered, we can observe that the basis *Meyer* wavelet has the best sensitivity while the *Mexhat* wavelet has the least. One significant advantage of using wavelet for fault detection is that we can choose the basis wavelet according to application i.e. in this case we can choose the basis which fits to the IDD waveform of the golden circuit best.

B. Increasing Fault Covereage by Supply Voltage Variation

For analog circuits, the fault coverage of the supply current testing methods can be improved if it is possible to switch transistors between different regions of operations. Variation of supply voltage is an approach by which we can achieve some control over the behavior of the transistors, thereby increasing the fault coverage. Kilic et al. [1] and Somayajula et al. [10] have proposed two different strategies of supply current variation for better testability. We experimented with varying supply voltage to investigate the effectiveness of wavelet method under these circumstances. In table V, we present the sensitivity of the two current testing methods for several catastrophic faults when a ramp input is applied to the supply rails. We consider only first 8 frequency components for both the cases. The result demonstrates that for current testing schemes which use supply voltage variation for better fault coverage, wavelet is about 7 times more sensitive than DFT.

C. Measurement noise

Effect of measurement hardware error is an important factor to consider for fault detection especially for off-chip supply current monitoring [4]. Usually the measurement hardware acts as a low pass filter smoothening out many high frequency components. Hence, the detection technique which largely depends on the high frequency components, is not suitable for off-chip testing. In our experiments, we have shown that wavelet renders a more sensitive detection method than DFT when both use only lower frequency components of IDD for fault detection. This observation makes wavelet a more promising technique than DFT for off-chip testing.

D. Process Variation

Setting the threshold between faulty and fault-free responses needs to consider the manufacturing process parameter variation. Time domain approach e.g. the charge integration is not very useful here due to problems like *aliasing*. We believe, wavelet components are better than DFT components for comparison of faulty and fault-free waveforms. The presence of timing and spectral information helps wavelet represent the true identity of the current signal better than what is possible in DFT based methods using only spectral components.

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TABLE III

EQUIVALENT NO OF COMPONENTS IN DFT FOR ISO-SENSITIVITY

Design	Fault	No of coefs (W av)	No of coefs(DFT)/ (Total Coefs)
LF	C4, -6s	4	74 (74)
	R5 open	4	59 (74)
	C3, +6s	4	74 (74)
	Vth, 10%	4	74 (74)
CTSV	C2 +6s	4	80(80)
	R5, +6s	4	43(80)
	R7, -6s	4	75(80)
	R6, +6s	4	70(80)

TABLE IV

VARIATION IN SENSITIVITY WITH DIFFERENT *mother wavelets*

Fault	mother wavelet	RMS	NormRMS
C1, +6s	Db2	1829709	6.654
	Meyer	1642714	31.739
	Mexhat	2104196	5.082
	Haar	1784817	11.198
R4, -6s	Db2	333998	2.083
	Meyer	316531	16.164
	Mexhat	398779	1.260
	Haar	322134	2.344

VII. Summary and Conclusions

Wavelet decomposition based dynamic supply current analysis has been shown to have better sensitivity than pure DFT or time-domain analysis method. This can be attributed to the property of wavelet transform to decompose the IDD signal in multiple resolutions keeping the timing information in place. Better sensitivity can help us get better fault coverage than pure spectral analysis for detecting parametric faults. Wavelet is particularly useful for off-chip analysis of IDD, because high frequency components of the current are usually filtered out by the measurement hardware and wavelet can approximate the residue signal better than DFT. Another important advantage of using wavelet over DFT is that we can use the *mother wavelet* to adapt to the current waveform of the particular circuit, producing better representation of the signal in terms of transform components. This is not possible with Fourier transform which has a fixed sinusoidal basis function.

Wavelet can be used for specification based testing as well. We believe, specification of an analog circuit e.g. the gain-bandwidth product can be better modeled by wavelet components because wavelet can better represent measured signal than DFT. Our research has also shown [12] that wavelet is very promising for fault detection in CMOS digital circuits too. This makes it a suitable candidate for testing Mixed-signal circuits with a unified testing solution for both digital and analog parts. Since wavelet can resolve events in time and frequency domain simultaneously, we can possibly use the timing information for fault localization. Currently we are exploring this possibility.

TABLE V

SENSITIVITY MEASURE FOR RAMP INPUT IN SUPPLY RAILS

Faults (Parametric)	RMS (Wav)	RMS (DFT)	$NRMS$ (W av)	$NRMS$ (DFT)
R6, VEE bridge	23.12	38.85	6.601	1.283
M1 src/gate short, opamp4	36.07	60.76	10.440	2.000
M7 drn/gate short, opamp5	26.47	44.13	7.529	1.216
Rc open, opamp3	21.15	1.91	1.05	0.06
R8, VCC short	2322.33	139.12	23.34	4.39

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