POLYCRYSTALLINE SILICON CARBIDE NEMS FOR HIGH-TEMPERATURE LOGIC

T. -H. Lee[1], K. M. Speer[2], X. A. Fu[3], S. Bhunia[2] and M. Mehregany[2]*
[1]Department of Materials Science and Engineering,
[2]Department of Electrical Engineering and Computer Science,
Case Western Reserve University, Cleveland, Ohio, USA
[3]Department of Chemical Engineering, University of Louisville, Louisville, Kentucky, USA

ABSTRACT

We report the first ever silicon carbide (SiC) nano-electro-mechanical systems (NEMS) switches capable of operation from 25 to 600 °C. We have developed both laterally- and vertically-actuated designs with threshold voltages of less than 5 V. Switches have been verified to cycle more than 3 billion times at room temperature and more than 2 million times at 600 °C. Plausible models to describe the contact resistance in two actuation voltage regimes are also suggested: (i) at low actuation voltage, the resistance is dominated by the native oxide which forms on the SiC surface; and (ii) at higher actuation voltages, the resistance can be described by Sharvin's model.

KEYWORDS

Silicon Carbide, NEMS, High Temperature, Contact Resistance

INTRODUCTION

Because of their potential to eliminate OFF-state power losses, switching systems based on NEMS devices are of recent and broad interest as an alternative to comparatively leaky electronics-based circuits – especially at elevated temperatures, where leakage current increases expeditiously. Unlike conventional electronic switches, leakage current in the OFF state of the NEMS switch is eliminated since its conductivity is based on the presence of physical contact. Such an all-mechanical logic capable of high-temperature operation also opens a pathway toward high-temperature computing.

Silicon carbide (SiC) is considered a strong candidate for NEMS switch technologies that demand performance at high temperatures and in harsh environments [1]. Specifically, polycrystalline (poly)-SiC holds valuable advantages over polysilicon, silicon-germanium, and common integrated circuits (IC) metals. First, for the same geometry, poly-SiC nano-beams have a resonant frequency that is 25% to 80% higher than polysilicon (based on the higher elastic modulus of poly-SiC); silicon-germanium and common IC metals are inferior to polysilicon in this respect. Second, poly-SiC is mechanically robust and chemically inert, enhancing long-term operational reliability. In addition, SiC has fewer problems with stiction, hence operational reliability is further improved. Finally, SiC's excellent electrical and mechanical stability at elevated temperatures extend the operational temperature regime to 600 °C – and possibly beyond.

This paper presents the design, development, and characterization of SiC NEMS switches with 75 nm gaps for just such applications. Switch reliability as a function of temperature and the physics of contact resistance in these NEMS switches are centrally discussed.

NEMS SWITCH DESIGN AND FABRICATION

Laterally- and vertically-actuated switch topologies, both with nanometer-scale gaps, have been designed and fabricated (Fig. 1). Among other factors, the performance of NEMS switches critically depends on the device dimensions. Operating voltage and switching time can be adjusted with appropriate scaling of the actuated beam's length and thickness – and to a lesser degree, the overlapping area of opposing surfaces that engage in actuation.

The fabrication process for the vertically-actuated switches (Fig. 2(a)) uses a silicon wafer whose topside is electrically isolated with a silicon nitride film. Atop the nitride film, the switch's bottom electrode is formed by LPCVD of a nitrogen-doped poly-SiC film [2]; the film is subsequently patterned with reactive-ion etching. The actuation gap is determined by the sacrificial release of ~75 nm-thick SiO_2 layers grown using thermal oxidation of the poly-SiC bottom electrode. A 100 nm-thick poly-SiC film is then similarly deposited and patterned to form the 10 μm-long, 5 μm-wide, 100 nm-thick beam that, after a sacrificial release of the oxide, serve as the switch's second electrode. To avoid stiction with these very small actuation gaps, vapor HF and supercritical releasing are used instead of the conventional BOE or HF etching.

For laterally actuated switches, a 1.5 μm-thick sacrificial SiO_2 layer is grown thermally on a silicon wafer, and the solitary poly-SiC layer is deposited to a thickness of 400 nm in the same process as above. A 40 nm-thick Ni hard mask is evaporated and patterned using electron-beam lithography and a metal lift-off. Actuation gaps of less than 100 nm are obtained on the lateral switches (Fig. 2(b)) after the SiC dry etching process. A wet etch is performed to remove the Ni mask, and the devices are supercritically released.

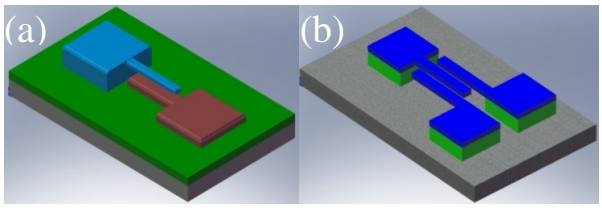

Figure 1: Schematics of the (a) vertical and (b) lateral SiC NEMS switches.

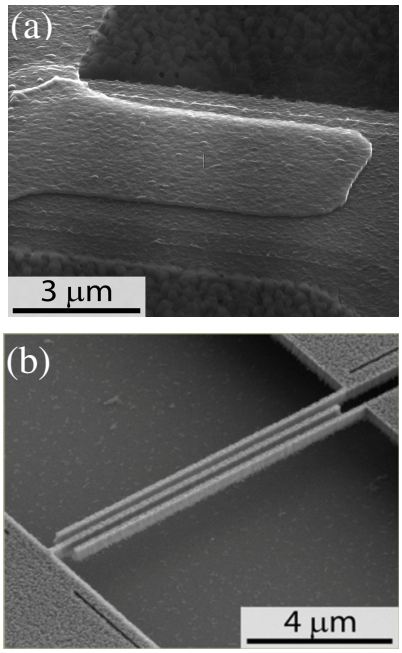

Figure 2: SEM photos of SiC switches: (a) vertical design with ~75 nm gap between top/bottom electrodes; and (b) lateral design with 200 nm-wide and 400 nm-thick beams, and 200 nm gap.

NEMS SWITCH CHARACTERIZATION

DEVICE OPERATION

Temperature testing was performed on a probe station with a customized hot stage (up to 400 °C) and on a ceramic package in a tube furnace (up to 600 °C), all at atmospheric pressure. Switches were cycled more than 3 billion times at room temperature and more than 60 million times at 400 °C. Additionally, a 10 µm-long vertical switch was actuated more than 2 million times at 600 °C at a frequency of 10 KHz before the aluminum bonding wire failed.

The threshold voltage, $V_{TH,}$ (defined as when detectable current passes through the switch) was 10-15 V for the first several cycles; subsequent cycles, however, exhibited V_{TH} of less than 5 V – a value that was maintained at elevated testing temperatures (up to 600 °C), as can be seen in Fig. 3. We believe that after the first several cycles, the native oxide layer on the SiC surface undergoes soft dielectric breakdown, resulting in a finite resistance and measureable current flow at lower V_{TH}.

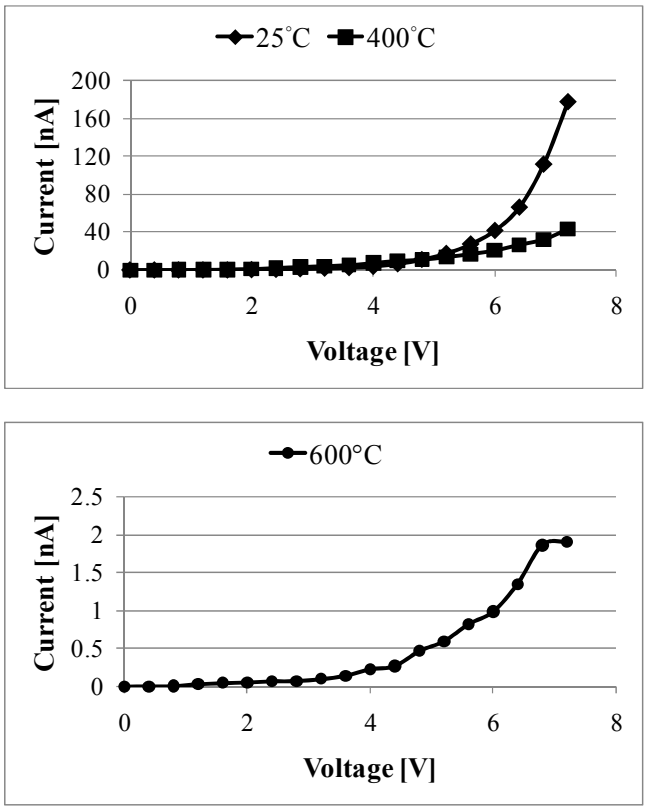

Figure 3: I-V characteristics showing (top) room temperature and 400 °C operation and (bottom) 600 °C operation.

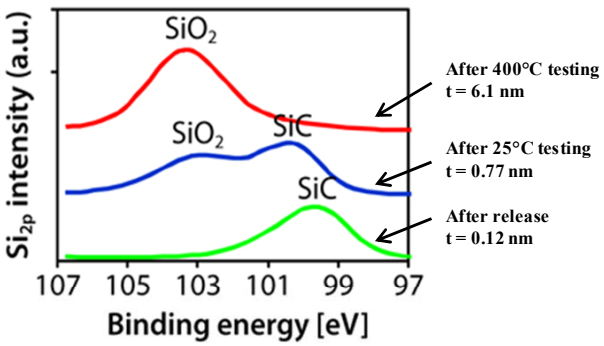

Figure 4: XPS data showing the evolution of native oxide on the poly-SiC surface with increasing temperature.

X-ray photoemission spectroscopy studies (Fig. 4) revealed that a 1 nm-thick native oxide layer is formed on the poly-SiC surfaces—and thus, the device— during exposure to a room-temperature air ambient. The thickness of this native oxide layer increases with increasing measurement temperature. The thicker oxide layer results in a lower switching current at elevated temperatures, as can be seen in Fig. 3.

CONTACT RESISTANCE

Extracted from Fig. 3, for a 10 μm-long switch the contact resistance is about 5 MΩ at 10 V and 2 MΩ at 15 V after the first few cycles, which is higher than that for common metal-based switches [3]. In mechanical switches, the contact resistance depends primarily on: (i) the materials coming into contact; and (ii) the radii of contact asperities (r_C). With regard to (i), the native oxide layer (discussed in the previous section) dramatically increases the contact resistance. As for (ii), the contact force increases with increasing actuation voltage, resulting in a lower contact resistance, as shown in Fig. 5.

The radii of contact asperities can change with contact force and the material's hardness [4]. Since the calculated contact radius of the asperities is smaller than the mean free path for electrons in SiC, instead of the well-known Maxwell spreading resistance, Sharvin's model [5] is instead used to calculate the contact resistance, R_C:

$$R_C = \frac{4\rho l}{3\pi r_C^2} \qquad (1)$$

where ρ and l denote the resistivity and the electron mean free path of the contact material, respectively.

At higher actuation voltages (12 to 17 V), Sharvin's model fits the experimental data well (Fig. 6); for actuation voltages less than 10 V, however, calculated contact resistance values are much lower than measured values. We believe that at lower actuation voltages, the surface native oxide resistance (R_{OX}) still dominates, even though the oxide has undergone soft breakdown. At higher actuation voltages, the post-breakdown native oxide behaves like a voltage-controlled resistor, following a power law [6]. R_{OX} can be neglected, then, and the contact resistance is determined purely by the contact asperities and materials.

Contact resistance can be expressed in terms of the contact force, F [7],

$$R_C \propto F^{-b} \qquad (2)$$

Using the Holm contact model [7], b = 1/3 and 1/2 when contact asperities undergo elastic and plastic deformation, respectively. The b value approaches unity when the contact force is sufficiently large, and the contact resistance is dominated by surface condition of the contact material. As depicted in Fig. 7, the b value is very close to 1, suggesting that the contact resistance in this region (voltages greater than 20 V) is determined by surface contamination, i.e., native oxide.

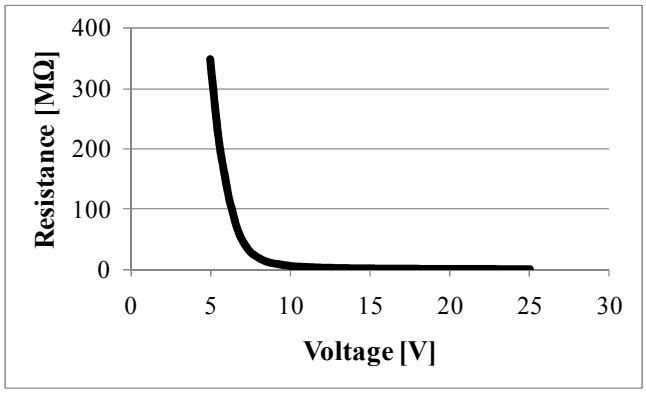

Figure 5: Contact resistance as a function of applied voltage.

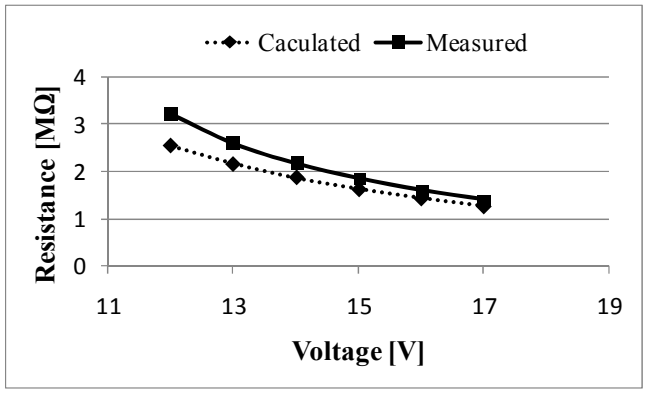

Figure 6: Comparison of measured contact resistance with those calculated using Sharvin's model.

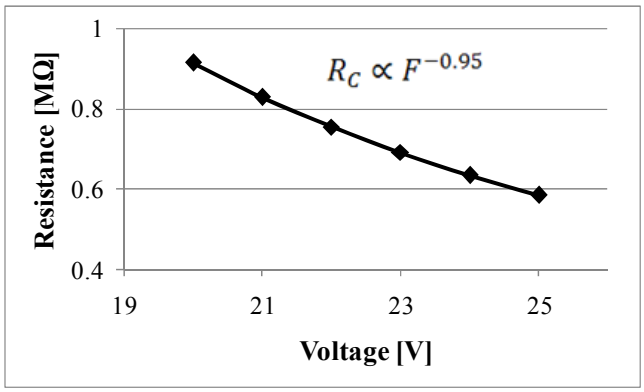

Figure 7: Contact resistance can be expressed in terms of contact force. For voltages higher than 20 V, contact resistance is almost inversely proportional to contact force.

LOGIC GATES DESIGN

For CMOS-like logic implementation using NEMS switch, a multiple-terminal device structure is required for independent gate control. We have very recently designed and patterned three-terminal laterally-actuated switches and split-gate structures with ~100 nm actuation gaps, as shown in Fig. 8(a) and Fig. 9. Basic examples of using these NEMS switches for logic applications are inverting and OR operations.

The inversion operation in the device of Fig. 8(a), which is schematically illustrated in Fig. 8(b), is achieved by (1) tying the gates (i.e., the input) of two NEMS switches together; (2) tying the drains of the two NEMS switches together; (3) the source of one of the two switches to V_{DD}

(HI), and (4) the source of the other switch to V_{SS} (LOW). When the input is HI, the cantilever beam of the switch whose source is LOW contacts V_{out}, resulting in a LOW output. If the input is LOW, the beam of the switch whose source is connected to V_{DD} contacts V_{out}, resulting in a HI output. The logical OR operation can be performed using the split-gate structure shown in Fig. 9. If one considers only one side of the terminals, (the other side is for use as an active pull-off in the case of stiction), it can be seen that a complementary input (i.e., HIGH if S is LOW or LOW if S is HIGH) to either G1 or G1' would actuate the cantilever beam into contact with D1, resulting in an output of whatever value the source holds. Thus, the basic OR operation is achieved.

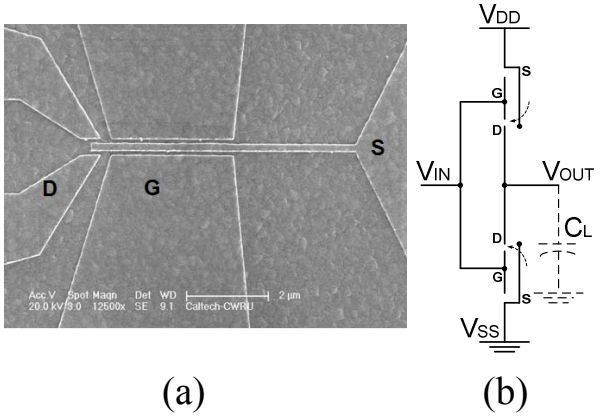

Figure 8: (a) SEM picture of the E-beam patterned three terminal switch and (b) schematics of the inverter using NEMS switches.

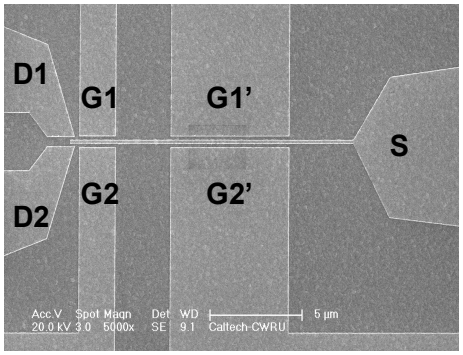

Figure 9: SEM picture of the E-beam patterned split-gate SiC switch.

CONCLUSION

Two different topologies of SiC NEMS switches, both with threshold voltages less than 5 V, have been fabricated and shown to operate more than 3 billion cycles at room temperature and more than 2 million cycles at 600 °C, the latter before the bonding wired failed. At low actuation voltages, the contact resistance of the switch is dominated by the native oxide layer on the SiC surfaces; at higher actuation voltages, the contact resistance closely follows Sharvin's model. At high actuation voltages, the post-breakdown resistance of the surface native oxide can be neglected and the contact resistance is determined by the contact force (i.e., actuation voltage) and the radii of asperities on the contact surfaces.

ACKNOWLEDGEMENT

The authors thank the National Nanotechnology Infrastructure Network at the Pennsylvania State University for the e-beam patterning of the device in Fig. 2(b). We are also grateful to Professor Roukes' group at the California Institute of Technology for their advice and support in fabricating the devices in Figs. 8-9. This research is supported by DARPA Grant # N66001-07-1-2031.

REFERENCES

[1] V. Srikar and S. Spearing, "Materials Selection for Microfabricated Electrostatic Actuators", *Sensors and Actuators A*, vol. 102, pp. 279-285, 2003.

[2] X. Fu**,** J. Dunning, C. Zorman and M. Mehregany, "Polycrystalline 3C-SiC Thin Films Deposited By Dual Precursor LPCVD For MEMS Applications", *Sensors and Actuators A*, vol. 119, pp. 169-176, 2005.

[3] J. Schimkat, "Contact Materials for Microrelays" in *11th IEEE International Conference on Microelectromechanical Systems*, Heidelberg, Germany, 1998, pp. 190-194.

[4] E. Kruglick and K. Pister, "Lateral MEMS Microcontact Considerations", *J. Microelectromech. Syst.*, vol. 8, pp. 264-271, 1999.

[5] A. Duif, A. Jansen and P. Wyder, "Point-Contact Spectroscopy", *J. Phys.: Condens. Matter.,* vol. 1, pp. 3157-3189, 1989.

[6] T. Chen, M. Tse, X. Zeng and S. Fung, "On the Switching Behavior of Post-Breakdown Conduction in Ultra-Thin SiO_2 Films", *Semicond. Sci. Technol.,* vol.16, pp. 793-797, 2001.

[7] R. Holm, *Electric Contacts*, Springer-Verlag, Inc., New York, 1967.

CONTACT

* T.-H. Lee, tel: +1-216-368-3051; tehaolee@case.edu