A Variation-Aware Preferential Design Approach for Memory Based Reconfigurable Computing

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***Abstract*—Static Random Access Memory (SRAM) arrays designed in sub-90nm technologies are highly vulnerable to process variation induced read/write/access failures. In memory based reconfigurable computing frameworks, which use large high density memory array, such failures lead to incorrect execution of mapped applications. It causes loss in Quality of Service (QoS) for Digital Signal Processing (DSP) applications. We propose a "Preferential Design" approach at both application mapping and circuit level, which can significantly improve QoS and yield under large parameter variations. Such a architecture/circuit co-design approach can also tolerate increased failure rate at low operating voltage, thus facilitating low-power operation. Simulation results for a common DSP application show 45% improvement in power at iso–QoS and 47% in yield for a target Peak Signal to Noise Ratio (PSNR) at 45nm technology.**

I. Introduction

Memory has been the fundamental building block for most of the popular reconfigurable platforms including the commercial Field Programmable Gate Array (FPGA) fabric. Recently a time-multiplexed Memory Based Computing (MBC) model has been investigated that uses dense 2-D memory array to map large multi-input multi-output LUTs [2-3]. In MBC, a target application is decomposed into a number of smaller functions (or partitions) which are evaluated in topological order over multiple cycles. Since MBC uses large, high-density memories for computation, reliable operation of the framework under increasing process variations becomes a major concern. Variation may potentially cause memory access failure or flipping of stored data during read-out [1], which leads to incorrect execution of the mapped application. Moreover, in order to reduce the power requirement, memory core is conventionally operated at lower supply voltages. Although this minimizes the active and leakage power consumption, memory read and access failure probabilities increase significantly at low operating voltages [1].

In order to compensate for variation-induced failures in memory, statistical design [1] along with built-in redundancy have emerged as a popular design choice. However, improving the yield for all sections of a large memory array can be extremely challenging due to within-die variation induced distribution of reliability across different memory sections. Therefore, a preferred solution for MBC would be to utilize different sections of a large memory block with different reliability in a way that minimizes the impact on performance. This can be achieved by exploiting the nature of the mapped applications. We note that computations in DSP applications can typically be classified into two categories: a) *significant components:* failure to compute them correctly leads to large loss in output performance; b) *less significant components:* any failure in these components cause considerably less impact in output performance. For example, in case of Discrete Cosine Transform (DCT), it is observed that 85% or more of the input image energy is contained in the first 20 of total 64 coefficients [4]. In order to achieve graceful degradation in QoS for DSP applications, we propose a *reliability map* aware application mapping methodology for MBC frameworks. The proposed methodology maps the critical computations to more reliable sections of the memory, and hence achieves maximum QoS under variations.

In addition, we note that MBC operation is dominated by read, while write only occurs occasionally during reconfiguration. Exploiting the read-dominant memory access pattern in MBC, we propose a preferential memory cell sizing approach that makes the memory more robust to read and access failures. The resultant decrease in write stability can be addressed by a column based lowering of the cell supply during reconfiguration. In particular, the paper makes the following contributions:

1) *It studies the effect of process variation induced failures on the performance and power for DSP applications in a time-multiplexed reconfigurable computing framework.*
2) *It proposes a reliability map aware mapping methodology for signal processing applications which can significantly reduce variation-induced output quality degradation without any hardware overhead.*
3) *It proposes a sizing based circuit level preferential design approach for memory cells which improves stability of read operation over write. This exploits read-dominant access pattern in MBC to improve output quality.*
4) *It evaluates the effect of the proposed circuit-architecture co-design approach on QoS, power, and yield for a common DSP application namely DCT.*

II. Overview of Memory Based Computing

Fig. 1 illustrates the memory based reconfigurable computing framework. Information regarding the address, scheduling steps and connectivity among the partitions is stored in a register bank (denoted as *schedule table* in Fig. 1) during the application mapping phase. The logic partitions obtained from the partitioning step are mapped to an embedded memory array, referred as the *function table*. In an evaluation cycle, a bank of flip-flops interfaces with the memory array to store intermediate partition outputs. The schedule table, the function table and the intermediate register bank form the core of the computational building block, referred as Memory-based Computational Block or *MCB* in the proposed framework. Multiple MCBs communicate through a reconfigurable interconnect framework similar to conventional FPGA.

To illustrate the effect of process variation on the memory based reconfigurable framework, the DCT architecture as described in [4] was mapped to the MBC framework. The resolution for each input

ICCAD'09, November 2–5, 2009, San Jose, California, USA.

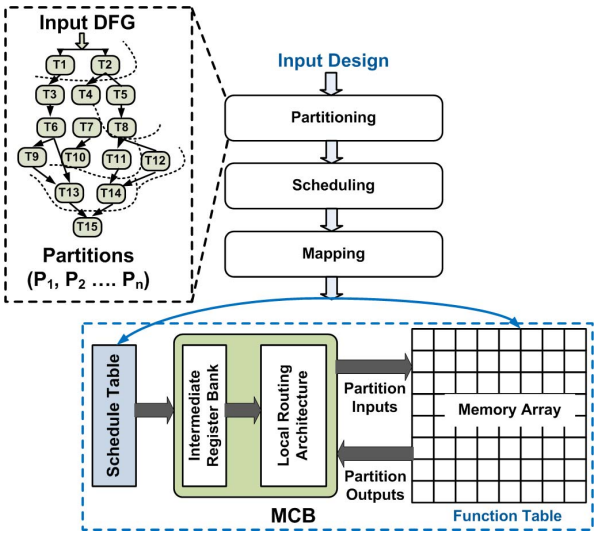

Fig. 1. Functional block diagram of Memory Based Computation.

from x_0 to x_7 is taken to be 8 bits and LUT at each MCB is configured as 4-bit adder. 12-b addition is therefore completed inside each MCB in 3 cycles using folding transformation. The total memory requirement for the mapped 1D-DCT computation is 12KB. This includes contribution from i) Sum and difference generators (2KB), ii) pre-computers (multipliers) with reduced alphabet set (1.5KB) and iii) adders after the vector scaling stage (8.5KB). It is worth noting that depending on the adder stage affected by variation, one or more DCT coefficients ($q_0 \cdot \cdot q_7$) may be affected. However, as most of the input image energy is contained in the first few DCT coefficients ($q_0 \cdot \cdot q_4$), any degradation in the values of $q_5 \cdot \cdot q_7$ have little impact on the output image quality [4].

III. Effect of Parameter Variations on QoS

Random variations in process parameters can cause mismatch between adjacent transistors in a SRAM cell, which may eventually lead to parametric failure of the cell [1]. Major cell failure mechanisms include: i) *Access Failure*, ii) *Read Failure*, iii) *Write Failure* and iv) *Hold Failure*. Let us consider a memory model consisting of 16KB of memory, divided into 128 blocks, each with 1024 cells. The memory was organized into 32 rows (N_{ROW}) with 32 cells (N_{COL}) in each column. The number of redundant columns in each block (N_{RC}) is 2. We performed simulations with this memory using HSPICE for PTM 45nm LP models [5]. We considered the following scenarios:

1) Nominal, slow and fast corners considering 15% inter-die variation.
2) Cells across the blocks were assumed to suffer from spatially correlated variation with standard deviation $\sigma_{dVtsys} = 50mV$.
3) V_t fluctuations (due to random intra-die variation) in the 6T-SRAM cell were modeled as six independent Gaussian variables with $\mu = 0$ and $\sigma_{dVt0rand} = 50mV$ for minimum sized transistor.

From the Monte Carlo (MC) simulations performed on the cells inside each block, we noted the parameters V_{read}, V_{trip}, T_{access} and T_{write} for each cell. In order to quantify the vulnerability of individual memory blocks, we introduce block level reliability metrics obtained by collating V_{read}, V_{trip}, T_{access} and T_{write} parameters from individual memory cells. The metrics are:

- Indicator for Read Stability denoted as I($V_{trip} - V_{read}$)
- Indicator for Write-ability denoted as I(T_{write})
- Indicator for Access-ability denoted as I(T_{access})

In general the indicator $I(x)$ where $x \equiv V_{trip} - V_{read}$, T_{write} or T_{access} for a memory block can be derived by:

- Classifying the cells of the block into separate bins based on the value of parameter x
- Calculating a weighted average of the cells in each bin:

$$I(x) = \frac{\sum_{i=1}^{N} n_i * w_i}{\sum_{i=1}^{N} w_i} \quad (1)$$

In equation (1), w_i denotes the weight and n_i denotes the number of cells in the i_{th} bin. For our simulations,we have divided the cells in each block into 5 bins ($N = 5$) with $w_i = 2^{-i}$ values. The range of $x \equiv V_{trip} - V_{read}$ values for the bins are : i) $x \leq 0$, ii) $0 < x \leq 100mV$, iii) $100mV < x \leq 150mV$, iv) $150mV < x \leq 200mV$, and v) $x > 200mV$. $I(x)$ for a given block serves as an indicator of the process corner to which the block has moved due to systematic variation. A block with a larger value of $I(V_{trip} - V_{read})$ is more prone to read disturb failures under increased environmental stress (i.e. reduced voltage and or higher temperature). Fig. 2(a) shows the inter-block distribution of $I(V_{trip} - V_{read})$ at the fast corner. In order to see the effect of these failures on the final DCT output, LUTs for the DCT operation were first randomly mapped to the blocks of our memory model. Fig. 3 shows the output image quality for random mapping of the LUTs to the memory blocks. For the example RGB image (I) considered in our simulations (as shown in Fig. 3(a)), the PSNR for the image (K) at the DCT output is computed using the equation provided in [10]. As shown in Fig. 3(b), due to random assignment, the final image quality suffers considerable degradation with an average worst-case PSNR of 28.49dB.

To alleviate degradation in output quality due to variation induced memory failures in the MBC framework, we propose a three-step solution that involves joint circuit/architecture level optimizations. As summarized in Fig. 4, the major steps in the proposed co-design approach are:

- A preferential (skewed) design of memory cell using transistor sizing that increases the read stability at the expense of write failures for the read-dominated MBC framework.
- Post-fabrication characterization of the memory and generation of the reliability map to store $I(V_{trip} - V_{read})$, $I(T_{write})$ and $I(T_{access})$ values for the memory blocks.
- A preferential application mapping approach that maps the critical computations to more reliable memory blocks.

IV. Preferential Mapping

A number of techniques [7-9] have already been proposed to generate post-Si reliability map for embedded memories in order to cope with device variation induced parametric yield loss. These

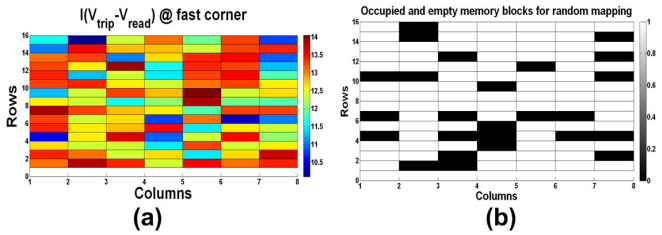

Fig. 2. a) shows the variation in $I(V_{trip} - V_{read})$ for the memory blocks at fast corner. (b) Random mapping of DCT modules to memory blocks.

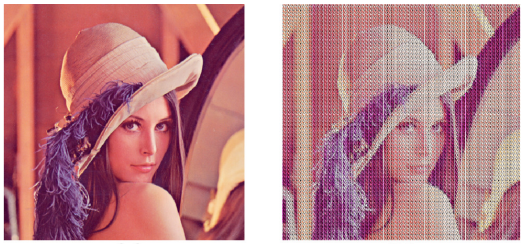

Fig. 3. (a) Original image at input of DCT; (b) Image after 1D-DCT (Average worst case PSNR = 28.49dB).

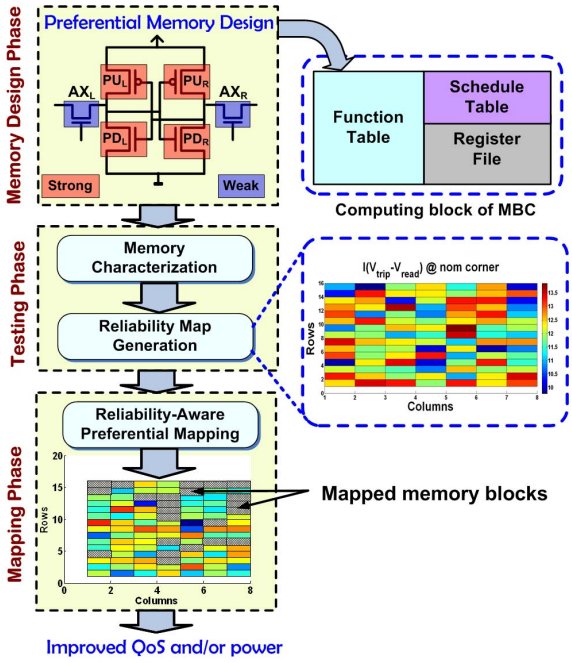

Fig. 4. major steps in the Proposed methodology for robust and low-power operation in MBC.

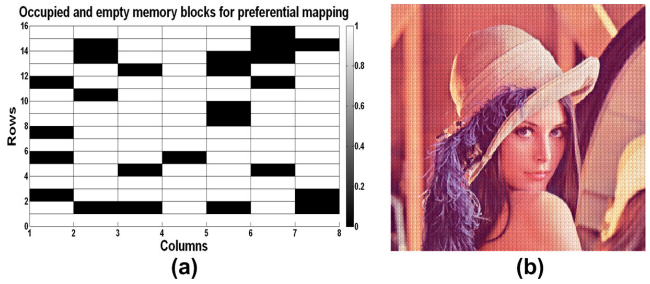

Fig. 5. (a) Preferential mapping of DCT modules to memory blocks (b) Image after 1D-DCT ($Avg_{PSNRwrst} = 32.48dB$).

techniques either use March Test [6] to detect parametric failures or attempt to directly measure the read/write margin for memory cells [7, 9]. We propose a heuristic-based preferential mapping approach that can substantially improves the output quality of the target application under parameter variation. If c_i(i=1··P) denotes the contribution of the i_{th} computation to the overall output quality and $r_i (i = \cdot\cdot N,\ N \geq P)$ denotes the reliability measure of the i_{th} memory block, then the mapping heuristic should attempt to maximize $\sum_{i=1}^{P} c_i r_i$. By reliability measure for the i_{th} memory block, we mean $r_i = \frac{1}{I_i(x)}$. The proposed approach is to sort $C = \{c_i\}$ and $R = \{r_i\}$ in descending order of their values, and then to assign the computations in the order of their contribution to unassigned memory blocks with highest value of r_i. Since probability of read failure (P_{RF}) dominates over the other parametric failure mechanisms at low frequencies of operation, the assignment of blocks have been based upon I(V_{trip} - V_{read}). Fig. 5(a) shows the memory block assignment using the preferential mapping approach. The unassigned memory blocks are highlighted in black. A comparison with Fig. 2(a) clearly shows that blocks with high $I(V_{trip} - V_{read})$ have been avoided through the proposed mapping approach. The output as shown in Fig. 5(b) achieves about 4dB improvement in PSNR over a random mapping policy.

V. Preferential Memory Design

A. Preferential sizing of 6T-SRAM

The criteria followed for preferential sizing of the 6T-SRAM cell are: 1) minimize the read/access failure probabilities; and 2) minimize the impact on cell area, which is estimated as in [1]. To exploit the read-dominant access pattern of the MBC framework, we propose to skew the memory cell for low read failure probability (P_{RF}). This is achieved by:

- Increasing width of the pull-up transistor (W_{PUP}) that increases V_{trip} and reduces P_{RF}.
- Decreasing width of the access transistor (W_{AX}) to reduce P_{RF}.
- Increasing the width of pull-down transistor (W_{PDN}) to compensate for increase in access failure probability (P_{AF}) due to weakening of W_{AX}.

First two optimizations increase T_{write} and therefore increases the probability for write failure (P_{WF}). The old and new value for the transistor sizes are given in Table I. With $L_{min} = 45nm$, the increase in area per cell is 2.5%.

B. Compensation for Increased Write Failure Probability

Since a higher wordline voltage degrades the half-select stability of the cells in the same row, we propose to use a column based lowering of cell supply to achieve better write-ability of the skewed memory cell. Supply voltage for the memory cell was reduced to 0.7V to improve T_{write} Table II shows the overall failure rate for the nominal design, the skewed design as well as skewed design with lower cell supply voltage for write. A skewed design with lower cell supply for write reduces the cell failure probability (P_F) by factor of 111.94.

TABLE I
Transistor widths for nominal and skewed memory cell

Cell	W_{PUP}(nm)	W_{AX}(nm)	W_{PDN}(nm)
Nominal	100	150	200
Skewed	125	125	220

TABLE II
Cell failure probabilities for $V_{ddnom} = 0.9V$

Cell	P_{RF}	P_{WF}	P_{AF}	P_F
Nominal	3.28e-8	6.66e-16	2.92e-14	3.28e-8
Skewed	2.93e-10	2.77e-12	2.22e-14	2.95e-10
Skewed w/ lower WR V_{dd}	2.93e-10	3.33e-16	2.22e-14	2.93e-10

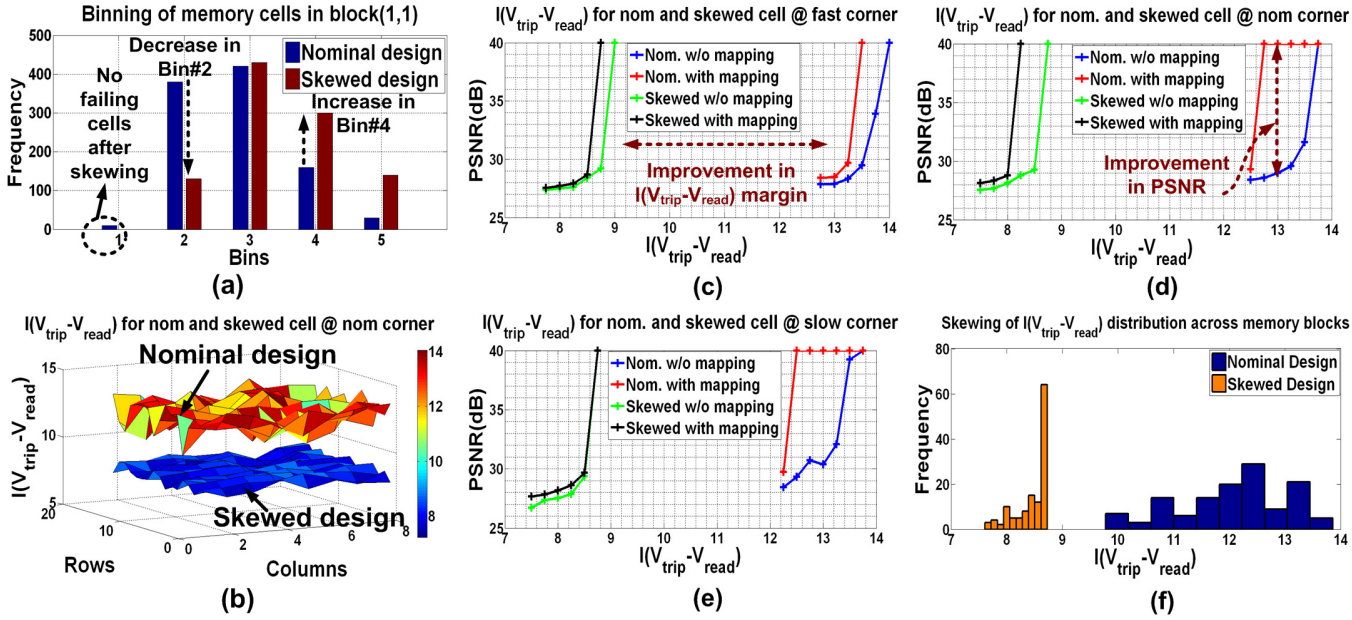

Fig. 6. a) Redistribution of memory cells into bins before and after skewing; b) Skewed design achieves better $I(V_{trip} - V_{read})$ for all blocks; PSNR values for i) original without mapping, ii) original with mapping, iii) skewed wi hout mapping and iv) skewed with mapping for c) fast, d) nominal and e) slow corners. f) Most blocks have moved to a similar $I(V_{trip} - V_{read})$ region after skewing.

C. Impact of cell sizing on output quality

The memory model as described in Section III was simulated with the skewed cell design for the same inter-die and intra-die variations. Fig. 6(a) illustrates the fact that skewing leads to redistribution of the cells in the 5 bins for a given memory block. Since a heavy penalty is associated with each failing cell, skewing leads to an improvement of $I(V_{trip} - V_{read})$ values across all the blocks in the memory (Fig. 6(b)). Fig. 6(c)-(e), illustrates the PSNR improvement achieved through the proposed preferential mapping and memory design. Following points may be noted from Fig. 6(c)-(e).

- A PSNR value of 40dB is used to represent a *no-degradation* case, although the PSNR is theoretically ∞ for no degradation.
- Preferential mapping for the original memory can achieve a significant improvement in PSNR for a range of $I(V_{trip} - V_{read})$ as high as 1.75. Considering that a cell moving from bin #1 to bin #2 reduces $I(V_{trip} - V_{read})$ by 0.25, this is equivalent to tolerating 5 more read failures in the memory block without increasing N_{RC}.
- Due to significantly smaller values of $I(V_{trip} - V_{read})$, the skewed design did not suffer from any degradation in output quality in our simulations. However, if the tolerance for $I(V_{trip} - V_{read})_{max}$ is reduced to smaller value (in other words considering a higher variation for the skewed design), a degradation of the PSNR values is observed at the output (Fig. 6(c)-(e)). Preferential mapping can again be applied to the latter case to improve performance.
- Improvement in output PSNR due to preferential mapping after skewing is comparatively smaller than the mapping applied to the original design. The reason for this is evident from Fig. 6(f) which shows that many memory blocks have comparable value of $I(V_{trip} - V_{read})$ after skewing.

VI. Conclusion

We have presented a circuit-architecture co-design approach for memory based reconfigurable computing frameworks to tolerate variation induced memory failures in case of DSP applications. Process variations create a distribution of memory reliability across different blocks of a large memory array resulting in a reliability map. Using the reliability map, the proposed approach performs application mapping in a preferential manner that maps most significant computations in more reliable memory blocks. Considering the read-dominant access pattern, we have also presented a preferential memory cell design approach using transistor sizing that improves reliability of read over write. The impact on write stability during occasional write operation can be addressed by existing approaches such as lower cell supply during write. Using a common DSP application, we show that the proposed approach can significantly improve QoS leading to higher yield, while enabling low power operation.

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