Multiple Scan Chain Design Technique for Power Reduction during Test Application in BIST

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Abstract

Multiple scan chain has been used in DFT (design for test) architectures primarily to reduce test application time. Since power is an emerging problem, in this paper, we present a design technique for multiple scan chain in BIST (Built-In Self Test) to reduce average power dissipation and test application time, while maintaining the fault coverage. First, we partition the scan chain into a set of smaller chains of similar lengths in such a way, that the total number of scan transitions in the scan chain is minimized. Then, we use a novel scan re-ordering algorithm in each smaller chain to further reduce the transitions. Experiments on ISCAS'89 benchmarks show up to 46.2% (average 24.4%) power reduction using the proposed technique, compared to the scan partitions given in the RTL description. Unlike previous approaches, our solution is computationally efficient and test-set independent and thus, can be effectively applied to large BIST circuitry.

1. Introduction

Power dissipation during test mode can be significantly higher than during functional mode, since the input vectors during normal mode are usually strongly correlated in contrast to statistically independent consecutive input vectors during testing. This causes increased switching activity in the circuit under test and may affect the reliability of the circuit, since the junction temperature and current density can be higher than the design specification of the chip. Zorian in [2] showed that the test power could be twice as high as the power consumed during the normal mode of operation. Moreover, parallel testing in System On Chip (SoC) to reduce test application time, results in excessive energy and power dissipation. Increased power dissipation during start-up and periodical on-line tests with BIST circuitry in portable devices is crucial for longer battery life. It is, thus, important on the part of the designers to ensure reduction in power dissipation during the test mode.

Several approaches to reduce power dissipation in scan circuits during test application have been proposed. Wang et al. proposed a new version of the path-oriented, decision-making (Podem) algorithm in [3], which minimizes the number of transitions. In [4], a test pattern generator is proposed, which reduces activity at the circuit inputs. Test vector inhibiting techniques have been proposed in [10]. Scan flop ordering techniques to reduce average power has been proposed in [1] and [11]. However, these techniques have either significant overhead of test application time/area [3, 4] or they are not computationally efficient [1, 14, 12] and therefore, cannot effectively be applied to large

circuits. Furthermore, most of these techniques [12, 14] are test set dependent and, hence, is not suitable for BIST using weighted random patterns.

Scan chain partitioning to reduce the test application time or to reduce the wiring overhead has been addressed quite extensively. However, multiple scan chain-based DFT architecture to reduce power dissipation has been practically unexplored. Nicolici et al. in [12] proposed scan chain-partitioning technique to reduce spurious transitions in the combinational part of the circuit. However, the authors did not address the problem of power reduction in scan flops, which is the principal source of power dissipation during testing. Furthermore, the solution in [12] is test-set dependent and hence, is not appropriate for using in BIST. The authors also propose another solution in [14] for scan chain partitioning to reduce power during shift and capture cycle and enable only one partition at each test clock. In [13] the authors presented a solution to reduce power dissipation during both shift and capture cycle but they assume that the partitions for multiple scan chains are provided. To our knowledge, there is no known previous work, which is directed towards optimal partitioning of scan chain to reduce the power dissipation during scan operations.

In this paper, we present a methodology to partition the scan chain for low power, which is suitable for application in Test-Per-Scan BIST circuits. In a BIST circuit, pseudo-random test patterns are usually generated by a Linear Feedback Shift Register (LFSR) and the patterns follow a pre-defined set of weights for each of the bits. Hence, test-set dependent power reduction techniques cannot be applied. We have used the weights of LFSR-generated patterns to design a simple graph-traversal based solution for low power multiple scan design problem. The solution works in two steps – first, we partition the scan chain into a set of smaller chains of near-equal lengths for optimal transitions in the scan flops and then, we re-order the elements in each scan chain to further reduce the total scan transitions. Experiments on ISCAS'89 benchmarks show that we can achieve up to 34% power reduction in scan chain by efficiently partitioning the scan chain, compared to standard partition as in RTL description and 46% power reduction by scan re-ordering. The algorithm incurs minimal overhead in test area and circuit performance and maintains desired fault coverage. The rest of the paper is organized as follows: Section 2 describes how the optimal weights for the LFSR are determined. Section 3 presents the proposed technique. Experimental results are presented in Section 4 for a set of benchmark circuits. Section 5 concludes the paper.

2. Determination of Optimal Probability Activity Set

For stuck-at-fault testability, the signal probabilities of the inputs need to be optimized such that the internal node signal probabilities are close to 0.5 to achieve high controllability and observability [16]. Signal probability $P(k)$ of a node k of a circuit is the probability that node k is logical one. The normalized activity $a(x)$ is the probability of the signal to switch within a clock period and is defined as: $a(x) = P(\{x(t-T)\overline{x}(t)\} + \{\overline{x}(t-T)x(t)\})$, where $x(t-T)\overline{x}(t)$ denotes a switching transition from one to zero, while $\overline{x}(t-T)x(t)$ denotes a switching transition from zero to one. It should be observed that the switching probability is proportional to the dynamic power dissipation during test. To optimize the inputs for low power dissipation, it is essential to simultaneously optimize the probability and the activities at the input. An intuitive explanation for this can be given with the following two sequences of test vectors applied to one input of a circuit under test: The first sequence contains m zeros followed by m ones: *0000…111*; the second sequence also contains m zeros and m ones, but occurring

alternately: *010101…01*. The two sequences have the same signal probability of $P(x) = 0.5$, and hence, they are equivalent in activating stuck-at faults. However, the signal activities (probability of switching) are quite different. The complex problem of optimizing probabilities and activities can be decoupled into two separate smaller problems: first, optimize signal probabilities for testability; next, determine optimal activities for minimum dynamic power without affecting the test length.

The optimal state input signal probability set can be obtained as described in [6]. In this paper, we use the general algorithm proposed in [7] and [8], and adopt a data structure similar to [9] to estimate signal probabilities and activities at the internal nodes of the circuit. The exact calculation of signal probability is NP-hard. Hence, we efficiently partition the circuit to trade-off accuracy versus time [8]. Given the optimal state input probability set, the state output signal probability set can be computed as outlined in [5]. The optimal signal activities are much smaller than those of conventional weighted random testing, resulting in much lower average power. Experiments on ISCAS85 benchmark circuits show an average power reduction by using this technique is as high as 73% (with test length reduction) [16].

3. Proposed Technique for Power Reduction

3.1 Partitioning into Multiple Scan Chains

The test application time in scan operations is dependent on the length of the scan chain and in the case of multiple scan chains, it is dominated by the scan chain with the maximum number of scan flops. Thus, it is essential to partition the scan chain in such a way that the difference in the number of flops among scan chains is at most one or two and is commonly referred to as the balancing condition. Although not considered here, given the layout information and the information of clock domains, geometric constraints can also be incorporated into our proposed technique.

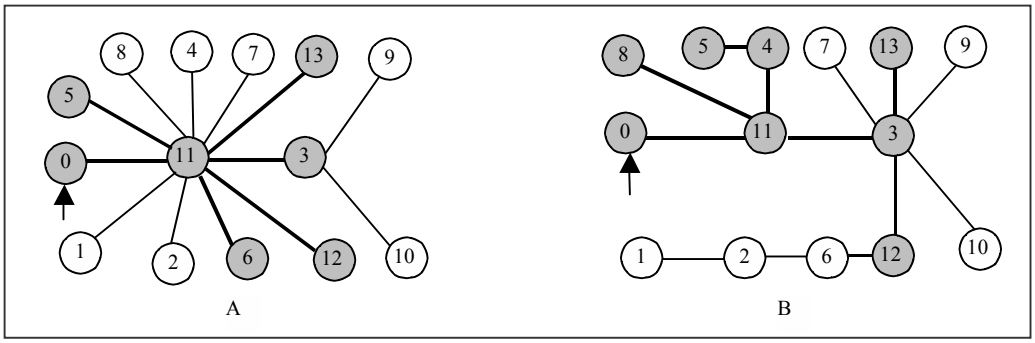

Fig 4. Example of tree traversal as dictated by the heuristic

To reduce the total power dissipation it is essential to assign each flop to a particular scan chain such that the total number of transitions in all the scan chains is reduced. Multiple scan chain optimization problem can thus be defined as follows: *Given a single scan chain of k scan flops, partition the scan chain such that the test application time is reduced to m (m<k), and the total power dissipated during scan operations is optimized.* Since a totally exhaustive search for finding the minimal cost partition is of exponential complexity and requires inordinate amount of computation, we resort to heuristics. We

propose a solution to the problem based on mapping the circuit as an undirected weighted complete graph *G(V, E)* where *V* is the set of scan flops, *E* is the set of interconnections between pairs of flops. The graph *G(V, E)* has a weight *w(u,v)* associated with each edge *(u, v)* in the graph. The edge weights are determined by the probability of transitions if the two flops are placed adjacent to each other in the scan chain. Thus, the problem can now be redefined as: *Given a graph G(V, E) with costs w(u, v) on its edges, partition the nodes of G into subsets of predetermined size so as to minimize the total cost of the edges.* The flowchart for the complete algorithm is given in Fig 5.

The proposed algorithm to partition the scan chain into multiple scan chains proceeds as follows: A global minimum of the edge weights that connects all the vertices is obtained by a Minimum Spanning Tree (MST). The MST was obtained by using the well-known algorithm proposed by Prim [15]. We use ISCAS'89 benchmark circuit, s298 to explain the proposed algorithm. The benchmark circuit, s298 has 14 flip-flops and our aim is to form two scan chains of seven flops each such that the total number of transitions in the two chains is minimized.

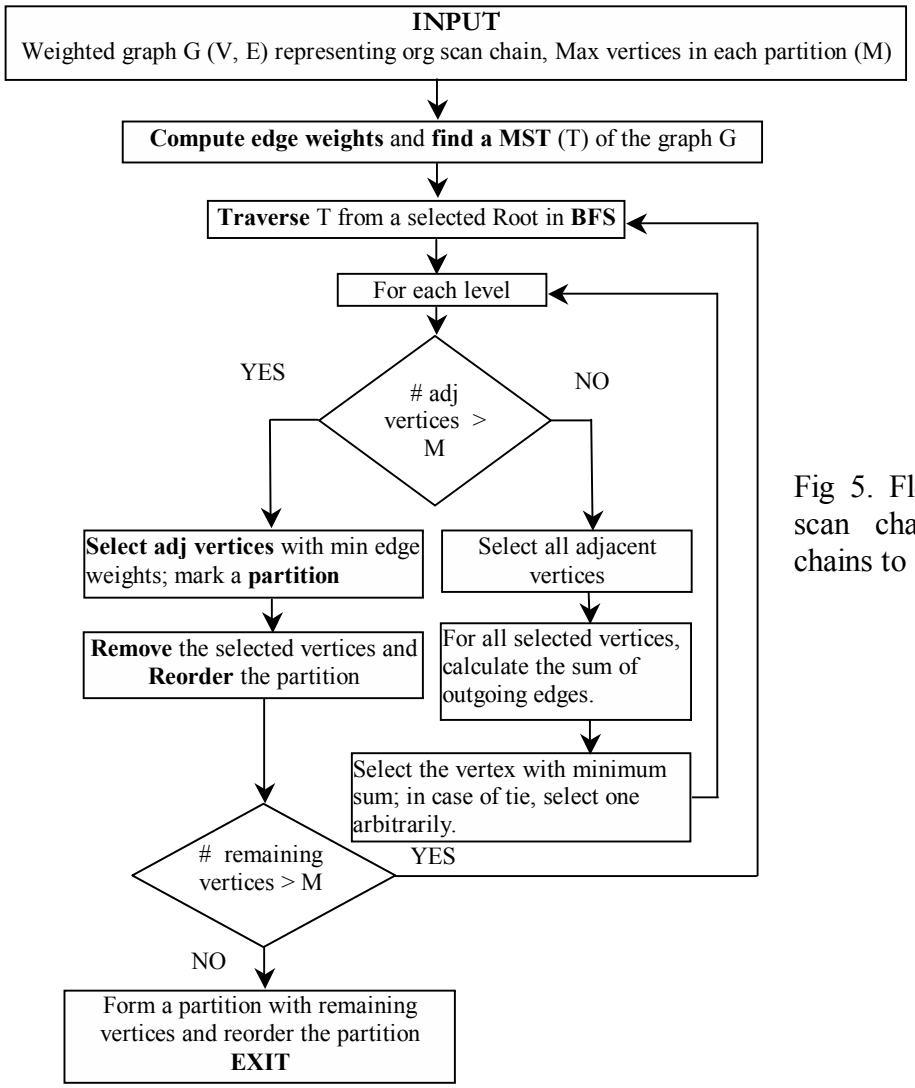

Fig 5. Flowchart for partitioning a scan chain into multiple smaller chains to minimize power

Fig 4 (A) shows the MST for ISCAS 89 benchmark s298. According to the proposed heuristic we traverse the tree based on modified Breadth First Search (BFS) as outlined below. We add the visited nodes in one set till we reach the upper bound on the number of elements allowed in one group. Any node can be selected as the starting node for tree traversal, (0 in this case, marked by an arrow in Figure 4 (A)). Since it has only one outgoing edge connecting it to node 11, we visit node 11 and include it in the set. The set now consists of two vertices {0, 11}. Thus, five more elements are needed to complete the set. Now we consider the unvisited vertices adjacent to node 11. Since node 11 has more than five adjacent vertices we select those vertices, which have the minimum edge weight, connected to node 11. The set formed is {0, 11, 3, 12, 13, 5, 6}. The remaining seven unvisited vertices form the other set. The two scan chains thus formed are subsequently re-ordered according to the ordering procedure mentioned in the following section. The last set formed using this procedure is not necessarily optimal, but since we form multiple smaller scan chains in this way and all but the last one is optimally chosen, we get substantial power saving.

If more than two scan chains need to be formed, we remove the visited vertices after the first iteration and then the remaining vertices are used to form a complete graph. An MST of the graph is constructed and then the scan chains are formed using the same procedure as outlined earlier. For the benchmark circuit s298 used as an example earlier, 3 scan chains of length 5, 5 and 4 are formed as follows: the first iteration results in the formation of a set of 5 elements {0, 11, 3, 12, 13}, the remaining vertices {1, 2, 4, 5, 6, 7, 8, 9, 10} are then used to form a complete graph and then the other 2 chains are subsequently formed.

Due to variation in the structure of the obtained MST, all circuits cannot be partitioned according to the procedure outlined above. We use the tree shown in Fig 4 (B) to explain the proposed heuristic. Again, we start traversing from any node, (0 in the present case, marked by an arrow) and since it has only one adjacent vertex we visit node 11. Thus, the set consists of two vertices {0, 11}. Node 11 has 3 adjacent vertices namely 8, 4 and 3. We need to form a set of seven elements and thus we include them in the set. The elements currently in the set are {0, 11, 8, 4, 3}. Two more elements are needed to complete the set of seven elements. To find the remaining two elements we find the sum of all the outgoing edges of the nodes visited last: node 8, 4 and 3 in the current case. In the present case, $\sum$ (all outgoing edges of node 8) < $\sum$ (all outgoing edges of node 4) < $\sum$ (all outgoing edges of node 3). Node 8 has no outgoing edges. Since node 4 has only one outgoing edge we select the vertex adjacent to 4, i.e. vertex 5. Thus, the set currently consists of {0, 11, 8, 4, 3, 5}. The last node added to the set is the vertex adjacent to node 3 with the minimum edge weight i.e. 13. Thus, the complete set of 7 vertices is {0, 11, 8, 4, 3, 5, 13}. The remaining elements form the other set. The two scan chains thus formed are subsequently re-ordered using the procedure outlined in the following section.

3.2 Scan In/Out Behavior Based Greedy Re-ordering Algorithm

We use a simple greedy technique to re-order the scan latches inside individual scan chains. Our approach is based on typical scan-in and scan-out behavior. If we observe the state of scan latches during scan-in and scan-out, we can easily identify how the transition patterns propagate through the scan latches. There can be three different kinds of transitions in a scan chain: transitions between two previous state bits, between previous state and new input bits, and between two new input bits. For each position of the scan chain, these three types of transitions will have different scope of propagation. In our approach, we select latches for different positions in the scan chain one by one in such a way, that it reduces the probability of propagation of scan transitions for that position. First, we

fix the first and last scan latches in the chain, then we go on selecting the second and the others from the available set of latches. It can be observed that, if m is the total number of latches in the scan chain and x is the position of the particular latch from the start of the chain, then previous state output value of any latch makes (m - (x-1)) transitions with respect to the previous state output value of the latch preceding it in the chain and (x-1) transitions with respect to the present state input. For a given set of previous state and scan input probabilities, we can easily determine the probabilities of transition in a particular latch.

This can be explained with the help of Fig 6, where L1 to L7 are scan latches, C1 to C7 are previous state outputs and B1 to B7 are present state inputs to be sequentially scanned into the scan chain. Fig 7 lists the various transitions possible and the corresponding number of times it can occur. It is evident that each of the scan latches (L1 to L7) can undergo maximum of seven transitions. Thus, in the above case there can be a maximum of 49 transitions during scan operation. If we can follow where the transitions occur, we can reduce them considerably. The scan latches can be arranged based on this information to reduce the number of transitions in the scan chain.

Cycle	L1	L2	L3	L4	L5	L6	L7
clk1	C1	C2	C3	C4	C5	C6	C7
clk2	B7	C1	C2	C3	C4	C5	C6
clk3	B6	B7	C1	C2	C3	C4	C5
clk4	B5	B6	B7	C1	C2	C3	C4
clk5	B4	B5	B6	B7	C1	C2	C3
clk6	B3	B4	B5	B6	B7	C1	C2
clk7	B2	B3	B4	B5	B6	B7	C1
clk8	B1	B2	B3	B4	B5	B6	B7

Fig 6. Transitions in different flops of the scan chain at different cycles

Latch	Trans from state X to state Y	# Trans	Trans from state X to state Y	# Trans
1	C1 and B7	7		
2	C2 and C1	6	B2 and B1	1
3	C3 and C2	5	B3 and B2	2
4	C4 and C3	4	B4 and B3	3
5	C5 and C4	3	B5 and B4	4
6	C6 and C5	2	B6 and B5	5
7	C7 and C6	1	B7 and B6	6

Fig 7. Particular transitions to account for when selecting a latch, and their weights

Fig 7 clearly shows that maximum number of transitions occur between the previous state output value of the first latch (C1) and the present state input value of the last latch (B7). Thus, we greedily fix the first and the last latch in the re-ordered chain such that the average number of transitions based on the output probability of the first latch and the input probability of the last latch is minimal. Once the first and the last latches are fixed, the rest of the latches are then placed incrementally one after the other in a fashion described below such that each time the total number of transitions is minimized. The search for the second latch proceeds as follows: there are 6 transitions between the previous state output value of second latch (C2) and the previous state output value of first latch (C1) and one transition between the present state input values of the second latch (B2) and the present state value of the first latch (B1). Thus, the second latch is fixed greedily based on the probability values such that the total number of transitions is minimized. Other latches are then subsequently placed to reduce this overall number of transitions.

The proposed technique can be applied for any scan-based design with no extra DFT logic. The fault coverage and the test length (time) are unchanged. It is a computationally efficient algorithm with complexity of $O(m^2)$, m being the number of latches and thus can be applied even for large designs.

4. Experimental Results

The above-mentioned algorithms have been implemented in C, and we obtain the optimal probability set using the method as described in Section 2. Fault simulation was performed using the HITEC/PROOFS fault simulator [17]. Simulations were run on ISCAS'89 benchmark circuits.

Table 1. Results of power saving using proposed technique

Ckt	# Scan flops	Fault Cov (%)	# Scan chains	Initial # trans in the scan chain	# Trans with multiple scan chain	# Trans with multiple scan chain (w/o re-ordering)	# Trans with multiple scan chain (with re-ordering)	% Improve	
								w.r.t org	w.r.t RTL des.
s298	14	98	2	45381	26219	17289	14355	68.3	45.2
s344	15	100	3	10415	4344	3365	3129	70	28
s349	15	99.4	3	9148	3962	3710	3561	61	10.1
s444	21	96.8	3	67261	23218	22101	20553	69.4	11.5
s510	6	98.9	1	18261	18261	18261	16381	11.5	11.5
s526	21	100	3	172888	83332	82520	73894	57.2	11.3
s713	19	93.3	3	519468	248493	231007	212526	59	14.5
s820	5	85.4	1	8931	8931	8931	8323	7.3	7.3
s838	32	73	4	888774	264989	222644	142492	83.9	46.2
s1423	74	97.7	4	1912607	655888	518625	456390	76	30
s1488	6	92.2	1	11542	11542	11542	10508	10	10
s5378	179	99.8	5	80846445	232116119	202654126	178335631	78	23
Avg								**70.8**	**24.4**

The experimental results are summarized in Table 1**.** The first and second columns show circuit name and the number of scan flops in the circuit. The third column refers to the fault coverage obtained. Since the signal probabilities are fixed, the test length and fault coverage is not affected. The fourth column refers to the total number of scan chains to be formed in the circuit. The fifth column shows the number of transitions in the original scan chain for the test-set generated using the algorithm outlined in section 2. Column six shows the number of transitions when the scan chain is partitioned as mentioned in the RTL description. The seventh column shows the number of transitions when the scan chain is partitioned according to the proposed partitioning algorithm. The eighth column shows the effect of re-ordering the multiple scan chains based on the proposed greedy algorithm. The % improvement is shown in column nine – the first half showing the improvement with respect to the original scan chain and the second with respect to the multiple scan chain formed as described in the RTL description. The average improvement is shown at the bottom of the table. Benchmarks with less than 10 scan flops were not partitioned, however were re-ordered according to the proposed technique, which reduced power dissipation.

Multiple scan chain results in large savings in power dissipation due to reduced rippling in the scan chain (average of 59.3% compared to original scan chain). However, optimally partitioned multiple

scan chains can further reduce power dissipation (average of 65.2% compared to original scan chain) with the proposed technique. Re-ordering the multiple chains also results substantial saving on top of the savings due to multiple scans (accumulating to an average saving of 70.8% compared to the original scan chain). Compared to multiple scan chains obtained from partitioning the scan flops as given in the RTL description, our procedure results in power savings up to 46.2% (average 24.4%) as shown in the right-most column. It is worth noting that the power saving percentage may be significantly higher compared to the worst possible partitioning and ordering of the scan flops.

5. Conclusions

The proliferation of portable devices has motivated research in the domain of low power testing. The paper presents an efficient low-complexity algorithm for average power reduction during testing using multiple scan chain based design methodology. Although the technique is test set independent and thus applicable to BIST, it can be easily extended to external scan testing. The proposed method gives promising power saving results with no significant design overhead in terms of area and performance.

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