NEMTronics: Symbiotic Integration of Nanoelectronic and Nanomechanical Devices for Energy-Efficient Adaptive Computing

Xinmu Wang, Seetharam Narasimhan, Somnath Paul, and Swarup Bhunia
Department of Electrical Engineering and Computer Science
Case Western Reserve University
Cleveland, Ohio, USA
Email: xxw58@case.edu

***Abstract*—Heterogeneity, programmability and parallelism are expected to be the key drivers for future nanoelectronics systems. The proposed work builds on these key drivers to achieve an energy-efficient, adaptive, and reliable computing framework. The primary intellectual merit of this effort lies in the heterogeneous integration of two fundamentally different state variables – charge-based electronics and electromechanical. We exploit the complementary capabilities of the two layers - high-performance operation of nanoscale FET and ultralow-power and harsh environment operation of NEMS – to merge the benefit of both. The layers are used in a symbiotic manner where each addresses the limitations of the other. The leakage/programmability issues in FET layer are addressed by exploiting the near-zero leakage and low ON-resistance of NEMS switches. The reliability and drivability issues of NEMS layer are addressed by FETs. The innovative memory based computing architecture exploits the density advantage of nanoscale memory to reduce the programmable interconnect overhead of traditional reconfigurable computing. It enables realizing custom computing functions in a core-based architecture to improve energy efficiency through hardware acceleration. The fundamental questions on the effectiveness of nanomechanical computing and the physics of its interaction with charge-based nanoelectronics are investigated.**

Keywords-Nanoelectronic, Nanomechanical, Hybridization, Energy-efficiency, Symbiotic Integration, High Temperature

I. INTRODUCTION

Future nanoelectronics are expected to enjoy the advantages of high integration density and improved switch performance. However, energy-efficiency and reliability of operation will continue to be major barriers to performance scalability and exascale integration [1]. Pervasive use of electronics in diverse applications will require reliable operation under widely varying operating conditions. For example, embedded automobile electronics is a rapidly growing market (with an expected electronics content of $2285/vehicle in 2013 [2]), which requires long-term operation at temperature 150-350°C. Similarly, many emerging applications of electronics in industry, marine, aviation, space and military require long-term operation in harsh environments. On the other hand, increasing use of electronics in biomedical applications e.g., implantable systems, will require working under ultralow power budget (e.g. <1 mw). Hence, future nanoelectronic systems should have the following major features: 1) high energy efficiency; 2) reliability under increasing error rates; 3) multi-functionality to adapt to diverse requirements (e.g. high performance or ultralow power); and 4) ability to work at harsh environments. Besides, they need to be developed at low engineering (design and test) cost with aggressive time-to-market.

The proposed research aims at achieving the above vision through heterogeneous integration of two computing layers, as illustrated in Fig. 1. It incorporates heterogeneous integration of: 1) nanomechanical and nanoelectronic computing devices; and 2) two different materials - Si (for nanoelectronics devices) and SiC (for nanomechanical devices), with the later being used for harsh environment computing. It also combines software and hardware programmability that enable realizing custom computing functions in a core-based architecture to improve performance and energy efficiency through hardware acceleration. Table I compares the major benefits and limitations of the two computing layers. The layers provide complementary capabilities, where nanoscale FET layer is effective for high to moderate performance computation, while the NEMS layer is effective for ultralow power and harsh environment computation (with reduced performance). Two layers enjoy a symbiotic relationship. The leakage/programmability issues in FET layer are addressed by exploiting the near-zero leakage and low ON-resistance of NEMS switches. The reliability and drivability issues of NEMS layer are addressed by the FETs. The NEMS layer also provides the opportunity to integrate sensor/actuators (e.g. mass detector, accelerometer) implemented with nanomechanical devices.

Contributions: The proposed symbiotic system architecture makes the following contributions through a set of cross-cutting research components. We explore efficient architecture, 3D integration techniques, and co-design approaches across abstraction levels to optimize the energy efficiency, reliability, and adaptability across ambient conditions and application demands.

1) *Energy efficiency and performance scalability (Von Neumann Bottleneck)*: The energy for a nanosystem is contributed by computation, memory access, data storage and

978-1-4577-0995-1/11/$26.00 ©2011 IEEE

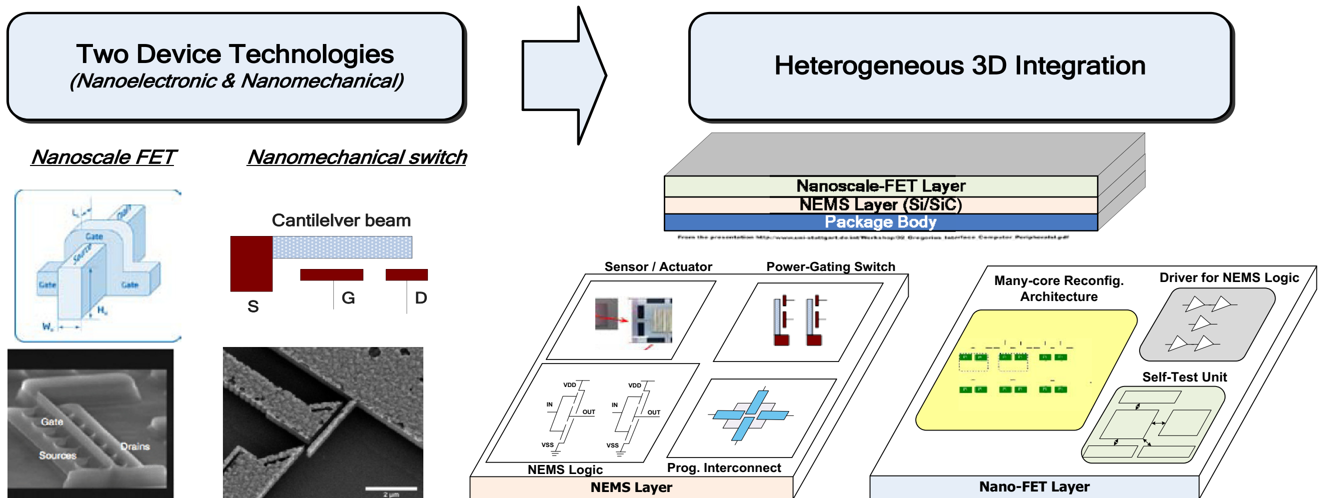

Fig. 1: The cross-cutting components, which combine alternate state variables (nanoscale FET and NEMS), heterogeneous 3D integration and a memory array based hardware reconfigurable computing fabric that exploits the high density of nanoscale memory and reduces interconnect overhead. [*Trigate image courtesy Intel Corporation].

data transport [3]. In particular, conventional von Neumann architecture of a processor spends significant energy in moving data between the computing resources and memory. Increasing energy consumption poses a major challenge to performance scalability.

2) *Heterogeneous integration*: Integration of two fundamentally different computing layers with different materials (Si and SiC) involves challenges in terms of electro-thermal interaction as well as pre- and post-bonding testing.

3) *Logic circuit design with NEMS*: Implementation of arbitrary logic and memory blocks involves major challenges due to lack of gain in the NEMS switches, which is a major barrier in multi-level logic and latch design.

4) *Reliability and testability of NEMS*: Due to their mechanical nature, NEMS switches are significantly more prone to run-time failure and various manufacturing defects. Hence, it is important to develop low-cost test and reliability solutions for the NEMS layer.

5) *Programmable hardware architecture*: Finally, conventional fine-grained reconfigurable hardware, such as FPGA, suffers from the performance/energy overhead due to elaborate programmable interconnect and provides poor technology scalability of performance. Hence, it is critical to develop a reconfigurable hardware architecture with better energy efficiency and scalability.

II. BACKGROUND

Due to the increasing demand for electronics for harsh environment e.g. high-temperature sensors, researchers have considered several device alternatives in the past. A notable effort in this regard is enhancing Si-based electronics using silicon-on-insulator (SOI) technology, which uses an insulator between substrate and transistor nodes, thus mitigating the problem of latch-up and high junction leakage at high temperature [4]. However, this technology fails to work reliably at temperatures above 300°C [5] and under high radiation. Bipolar ICs such as low-power Schottky (LS) or ECL devices can tolerate up to 10 Krad. Many applications however require tolerance to even higher doses [5]. Besides, these technologies suffer from large size and markedly increased leakage at high temperature.

Silicon carbide (SiC) has emerged as a promising semiconductor material for high temperature electronics because of its wide band-gap voltage (~3.3V, compared to 1.1V of silicon), high electric field breakdown and fewer crystal dislocation defects compared to other wide band-gap materials [5]. Several different SiC FET structures, such as SiC MOSFETs, Schottky-based metal-semiconductor FETs (MESFETs), and JFET have been investigated. However, poor gate oxide quality due to high oxide-Si interface trap density is a concern for SiC MOSFET devices, while the MESFET

Table I: Benefits and limitations of the two technologies of complementary nature

	Benefits	Limitations
Nanoelectronic Computing	• Terascale integration • High performance • High driving strength	• Large leakage • Threshold volt. scaling is limited by thermal voltage (K_BT/q) • Large overhead of prog. interconnects
Nanomechanical Computing	• Near-zero leakage • Possibility of ultralow threshold volt. → lower switching power • Robust operation at harsh-environments (e.g. at > 150°C)	• Low performance (limited by mechanical transition) • Lack of gain → lower driving strength • Low switch life-time

devices suffer from high gate leakage at high temperature. Among different transistor device structures, SiC JFET devices have been most promising in terms of manufacturability, device characteristics as well as large-scale integration capability. Reliable operation of SiC JFET based analog electronics such as amplifier has been demonstrated [6]. However, their large size, high threshold voltage and low switching speed make them unsuitable for logic design. In particular, multi-level cascaded logic design using these depletion-mode negative threshold devices has emerged as a major challenge. Besides, the high leakage current (both active and standby) through off transistors can cause huge power overhead at high temperature [7].

The use of NEMS switches has been widely explored for possible hybridization with CMOS electronics for minimizing leakage [8-9]. In [10], the authors introduced complementary NEMS switches made of Nickel, based on a tuning-fork structure and proposed several CMOS-like logic gate structures. A 4-terminal NEM-relay was presented in [11], along with a 32-bit full adder design using simpler logic style than static CMOS. The authors in [12] implemented FPGA routing using NEM-relays for low-power. A SiC NEM-relay based FPGA architecture is presented in [13] for high temperature applications.

III. System Architecture

We propose an adaptive system architecture that combines software and hardware programmability to achieve dynamic adaptation to application/environment requirements, while providing high energy-efficiency and reliability. Fig. 2 shows the overall system architecture. Software programmability is achieved by using a heterogeneous hierarchical multi-core architecture based on von Neumann computing model. Hardware programmability is achieved through spatio-temporal computing in memory using a memory-based computing model, introduced in [14]. The homogenous many-core architecture or co-processors (referred to as HRCP) provide tremendous parallel computing resources, which can be used for: 1) hardware acceleration, to realize custom functional units (e.g. signal processing or multimedia operations such as discrete cosine transform and filtering, security applications such as encryption and hashing); and 2) reliability improvement, to improve the reliability of operation through redundant computation in the parallel HRCPs. The core-based architecture is implemented in the nanoelectronic layer. The task scheduler runs in the core architecture, and decides when and how to use the reconfigurable hardware as well as when to transfer computation to the NEMS layer depending on application and environment demands. The central scheduler also manages data read-out and processing of the sensors and controlling the actuators in the NEMS layer. For harsh environment or ultralow power computation, the simple controller in NEMS layer takes over and manages computation in this layer. The sensors [15] are implemented in the NEMS layer for sensing change in temperature as the system is operated in a harsh environment. The two layers are implemented on different substrates/materials and connected through through-silicon vias (TSVs) [16] to form an integrated 3-D architecture. The symbiotic relationship between the two layers can be exploited to use the existing resources as testing, power-gating, driving, or interconnect structures when not in use for nanoscale computing. Next, we describe the different structures in the two layers and their intended functionality, as well as potential challenges.

System Integration: The hybrid implementation can be achieved by extending the existing silicon CMOS fabrication process. A possible integration solution, shown in Fig. 1, consists of separate layers for FET and NEMS, while an interconnect layer between these two layers makes the required connections between NEMS and FET devices. We contemplate a NEMS-last approach; otherwise the cost of CMOS fabrication would be high since a custom lot of whole wafers would be required. Post processing of CMOS chips from MOSIS, though inconvenient, is possible; the associated savings are significant. However, NEMS require deposition of poly-SiC at 800°C in on our current LPCVD poly-SiC technology. Even though the deposition time is quite short due to the thinness (e.g., several 10's of nanometers) of the NEMS poly-SiC films, the overall thermal budget is large because of the use of a hot-wall furnace, adding loading, unloading and ramping times at elevated temperatures. This of course is not an issue for the SiC logic circuits because diffusion in SiC at these temperatures is negligible, and high temperature metallization will be incorporated (i.e., we have control of the related baseline process development). One approach is to use PECVD SiC, which can be deposited at 400°C. However, we are concerned about the resistivity and mechanical properties of these films. In recent past, CMOS-compatible growth technique of CNTs, which also require high growth temperatures, has been widely investigated and several solutions have been proposed. However, our preference is to use a rapid thermal CVD (RTCVD) technology to eliminate thermal budget overhead associated with the furnace operation in the case of LPCVD. Doing so should make the thermal budget acceptable because of the thinness of the films.

IV. Nanoscale FET Layer

The nanoscale FET layer is intended as the current state-of-the-art silicon-based CMOS layer. At normal operating temperature, it serves as the high-performance primary computing resource. We envision the adoption of nanoscale memory structures due to their extremely high density and regular structure as an adaptive computing framework. This computing framework has also been shown to be portable to future-generation memory implementations using alternate device technologies. Since these device technologies suffer from reduced reliability, the adaptive computing framework is useful to ensure robustness of operation and portability to implement different logic functions on-demand. Apart from this, the FET layer also contains drivers and testing circuit for supporting the NEMS layer.

A. *Reconfigurable computing framework*

Use of embedded memory for computing to accelerate complex kernels in exascale systems provides several major benefits at different levels. Nanoscale devices are highly suitable for high-density regular memory array design. Besides, emerging non-volatile memory devices such as memristor, spin-torque RAM and phase change memories are very

promising for reconfigurable computing. Scaling trends reported by ITRS [17] predicts 10X improvement in integration density for memory compared to logic gates in future years. In addition, technological innovations such as "3D integration" suggest that future designs will have more than 60% improvement in on-chip memory speed, power and bandwidth. Besides, embedded memory provides large set of parallel resources with high bandwidth, which can be configured to perform computing in spatio/temporal manner. A possible µ-architecture of each HRCP would contain a memory array, a controller (Fig. 2) for sequencing lookup operations of functions stored in memory as lookup tables (LUT). The memory array (of typical size 4-16KB) will be organized into multiple parallel banks [14]. Each memory block will be augmented with a tiny controller to perform lookup operation from the memory. The operation of each HRCP is stored in micro-code format into a register file, called schedule table. The intermediate outputs will be stored in a small temporary register file (e.g. 8 16-bit registers). Time-multiplexed local routing will be used to select the operands in each clock cycle. Besides evaluation of complex functions using a LUT-based temporal execution model, the controller hardware will be capable of: 1) reading and writing data values from a subarray; 2) simple conditional control transfer; and 3) early termination of execution for a complex operation. The third capability is important for improving energy efficiency by exploiting the abundance of narrow-width operation in typical program, which allows terminating a 32-bit operation early if the effective size of both operands is 8, 16 or 24 bits.

B. *Drivers for NEMS Layer*

Since the NEMS switches suffer from lack of gain [13], they are expected to have drivability issues, which may prevent cascading a logic stage with another. We have observed this issue with our fabricated SiC NEMS switches [7]. In order to enable multi-level logic design using NEMS switches, we will investigate an approach where we insert buffer/repeater at strategic places in a NEMS logic circuit to boost its driving strength. For operation in normal temperature range (<150°C), these buffers can be made in the FET layer (as shown in Fig. 1). However, for high temperature operation, we plan to implement the buffers in the NEMS layer using SiC junction field effect transistors (JFETs) [6]. We select SiC JFETs here because poor gate oxide quality is a concern for SiC MOSFETs under high temperature and high electric field, while SiC MESFETs have high gate leakage [5]. The depletion mode JFET devices will be fabricated on a p-type, Al-doped 6H-SiC wafer with 3 epitaxial layers and realize buffers using them with an active resistive load.

C. *BIST for NEMS Layer*

At the system level, we will explore a ***self-test approach*** to detect both functional and parametric failures in the nanoelectronic and nanomechanical layers. The self-test approach will combine 1) a software-based test approach for autonomous testing of defects in the execution cores of nanoelectronic layer; and 2) a novel BIST mechanism for testing NEMS switches. The test hardware will be implemented in the nanoelectronic layer (as shown in Fig. 2) and will comprise of a test generation, a controller, and a response

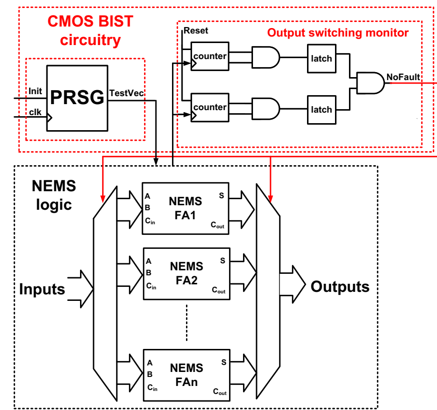

Fig. 2: CMOS BIST circuitry for a NEMS full adder.

analyzer unit. To improve test speed, the built-in self-test (BIST) unit will exploit the homogenous many-core architecture of the HRCPs to perform parallel testing of these cores. During testing, each HRCP core will be loaded with a set of micro-instructions which tests the memory block used by a specific core for all possible memory failures. We will initially use a standard MARCH test e.g. MARCH C- [18] for this purpose and then modify it based on the fault models in specific memory technologies to provide high defect coverage with minimal increase in test time. To detect failures in the controller logic in each HRCP, we will use a spatial cross-referencing approach, where the output of a test routine from multiple homogeneous cores will be compared with each other to identify potentially defective core. The approach can also be highly effective in fault localization, which can identify the core or a memory block inside a core, where a fault exists. Such a cross-referencing approach can also be used for performance calibration of each core under process variations. In this case, the operating condition (e.g. in terms of voltage or frequency) can be swept and the failure point for each core can be calibrated by comparing its output with neighboring cores.

The proposed hybrid framework provides a unique opportunity for self-testing the NEMS switches and circuits by implementing complex test structures in the nanoelectronic layer. From previous experience, we have observed the following major manufacturing defects in nanoscale mechanical switches: 1) the cantilever beam always touching the drain electrode (due to stiction); and 2) shorting of drain and gate electrodes; and 3) beam touching both gate and drain terminal on actuation. We will analyze these failure mechanisms in different NEMS switch structures both post fabrication and during operation under different stress conditions. Next, we will map the failure mechanisms to appropriate fault models. An important part of the self-test will be detection of stiction of beams by observing node activity. The unit will apply switching at the input of a logic block and monitor activity at the output. Aging induced failure in NEMS switches is expected to be detected by the activity monitor circuit. On the other hand, delay failure due to performance degradation can be identified by using a test structure in the BIST which latches the output of NEMS logic at a rated clock.

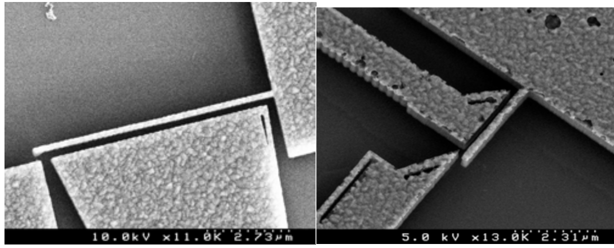

Fig. 3: SEM images of fabricated 3-Terminal NEMS switch. We have measured the switching parameters for the fabricated switches.

V. Nanomechanical Layer

A. Nanomechanical Logic

NEMS switches provide a unique opportunity to optimize the switch structures with minimal number of active elements for a specific function. It is important to reduce the number of active elements (i.e. cantilever beams) for multiple reasons: 1) it improves the performance, since NEMS logic performance is dominated by the mechanical transition time of the beams; 2) it improves the reliability, since less beams means less probability of run-time failures due to beam fracture or stiction; and 3) less die-area. Hence, we investigate custom switch structures for NEMS logic, programmable interconnects and power-gating of FET devices. In all cases, the near-zero leakage of NEMS switches will be highly beneficial. However, we will also try to minimize the ON-resistance (or ON-current) of the switches so that the performance overhead is minimized. Fig. 4 shows the structure of NEMS switches/circuits. Fig. 4a (middle) shows a laterally-actuated cantilever with 3 terminals of Gate (S), Source (S) and Drain (D). The on/off state of the switch is determined by the electrostatic force between the gate electrode and the source i.e. the cantilever [7, 13]. When a voltage greater than the cantilever pull-in voltage (Vpull-in) is applied at G with respect to S, the consequential electrostatic force will pull the cantilever and cause it to move towards the gate electrode, eventually making the beam end touch D and forming a conducting path between S and D. By sizing the beam/gate overlap and separation distance between beam/drain and beam/gate, it can be ensured that the beam never comes in contact with the gate, thus presenting large input impedance, similar in magnitude to the off-resistance of the switch. SEM of our fabricated NEMS switch is shown in Fig. 3

Based on this structure, more complex multi-gate switches have been derived to reduce the number of moving elements for certain logic functions. In particular, switch structure Fig. 4b is designed to turn ON only when both G electrodes exhibit potential opposite to that of S electrode, implementing an AND function. Since, simple NEMS switches lack independent gate control of the beam movement, which is critical for transmission gate and MUX design, one can design multi-layer beam structures (shown as switch structures Fig. 4c-e) to implement more complex logic functions with fewer moving elements.

The NEMS switches can be used to build complementary logic gates by using two different voltages at the source terminals of a switch to realize pull-up and pull-down logic structures as shown in Fig. 4, left. Since the electrostatic force will pull the beam towards the drain irrespective of the polarity of the voltage difference between G and S, this 3-terminal switch can be used as a pull-up or pull-down switch by connecting the S terminal to VDD or VSS. Thus, it can be used to construct static CMOS-type logic gates, like the inverter described in [7]. G electrodes of both switches are connected together as the input and D electrodes are connected as output. When logic ‘0’ (VSS) is applied at the input, the upper cantilever will be pulled-in to connect to D. The bottom cantilever will stay away from D under the repelling electrostatic voltage from G. As a result, D will have the same voltage as the upper relay after complete charging, meaning the output is logic ‘1’. Conversely, when logic ‘1’ (VDD) is applied at the input, the bottom switch will turn on and discharge the output to logic‘0’. Fig. 5(b) demonstrates the electrical model of the 3-terminal NEMS switch based on the behavior of NEMS cantilevers we fabricated. Cgs is the parasitic capacitance between G and S. The distributed beam

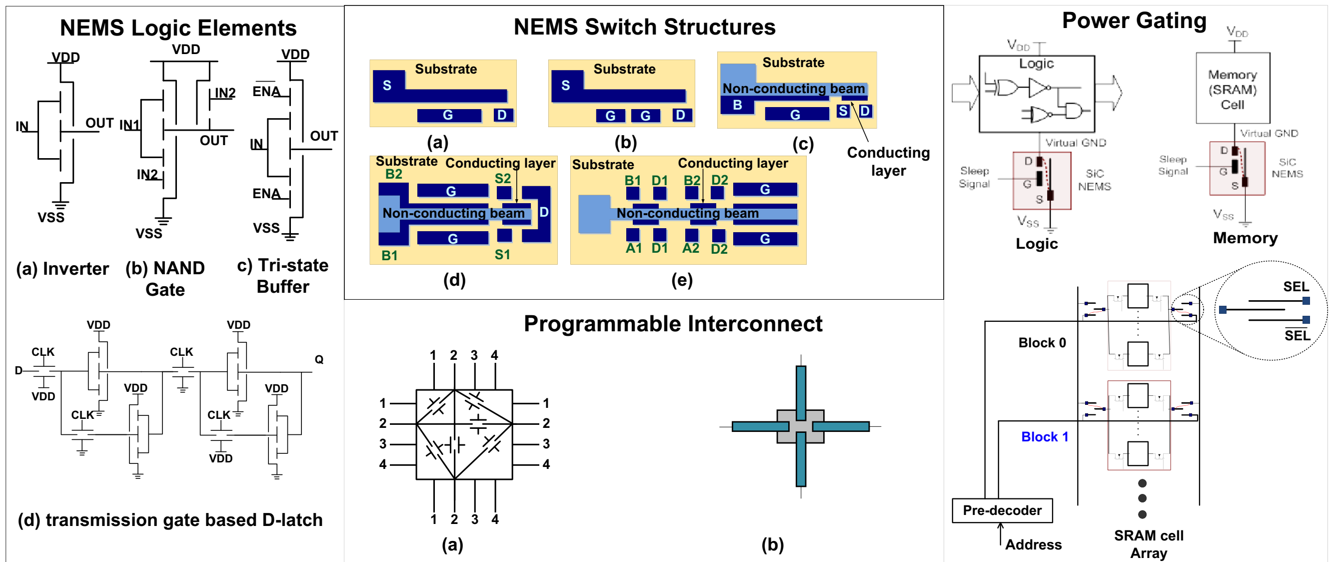

Fig. 4: NEMS logic elements, multi-terminal switch, 6 and 4-way programmable interconnects, and power gating structures.

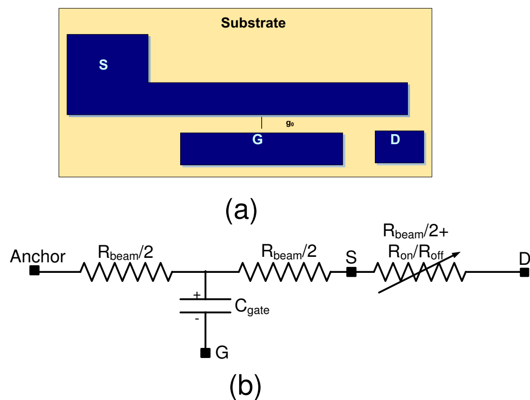

Fig. 5: (a) 3-T NEMS switch; (b) R-C electrical model [13].

resistance is represented by two resistors of value Rbeam/2. Resistance between S and D depends on the on-/off- state of the switch, which is determined by the voltage (Vgs) across Cgs. If |Vgs| is less than Vpull-in, the switch is in its off-state. The open circuit between S and D can be modeled with an off resistance Roff, whose magnitude determines the leakage current flow through the gap due to tunneling effect. Based on the experimental result of the tunneling current provided in [7], we set R_{off} to be $10^{15}\Omega$. Once the cantilever is pulled-in, the switch is in its on-state and resistance between S and D is the contact resistance between beam end and D. This contact resistance is represented by Ron in the model, which is typically much larger than the beam resistance [7]. Therefore Rsw can be modeled as a voltage-controlled resistor.

B. *Leakage Reduction of FET Layer*

Similarly, these NEMS switches can be used as power gating elements for CMOS-based logic to reduce the leakage [8-9]. Although the NEMS switches can be slower than MOS switches, once turned ON, they can provide a low-resistance path to ground, whereas, in the OFF state, they can be used to reduce leakage current due to absence of any conducting path between the beam and the drain. NEMS switch based power gating elements are illustrated in the right part of Fig. 4. A single switch of type (a) and a MUX based on switch type (d) can be used as power gating switches for logic core and memory cells, respectively. For memory power-gating, the switch must ensure that the virtual ground/supply is lower/higher than the Data Retention Threshold in the sleep mode. Similarly, the power gating switches can be deployed between local and global bitlines to turn off unused blocks of the memory (SRAM) array to reduce bitline leakage (Fig. 4, right bottom).

C. *Programmable Switches for Nanoscale FET Layer*

Besides basic digital logic elements, NEMS switches are also promising candidates for building programmable interconnects, for hardware reconfigurable frameworks [11-13]. Single-beam and multi-beam structures can be designed to create multi-terminal dense switching networks. A simple way of implementing a 6-way connection between four terminals is shown in Fig. 4 (middle bottom), where each possible connection is implemented using a transmission gate type switch. The other structure shown in Fig. 4 contains less switching elements and can be used to create 4-way connections.

VI. SIMULATION RESULTS

Based on the electrical model shown in Fig. 5(b), we build HSPICE netlist for ISCAS85 and ISCAS89 benchmark circuits and perform simulation on them using Synopsys HSPICE. Simulation results are shown in Table II. From these results we can see that leakage current of NEMS FPGA at 500ºC is about 100,000X lower than that of CMOS FPGA at room temperature, due to the electromechanical nature of the NEMS switches. Since the scaling of NEMS switch is not subject to the limit of thermal voltage (K_BT/q), it is a promising option for ultra-low power high-temperature applications in terms of scalability. The results also show that transition energy of NEMS FPGA is comparable to that of CMOS FPGA. When it comes to active area and critical path delay, NEMS switch based circuits are considerably worse than CMOS circuits. However, since the NEMS circuit delay is mainly contributed by the mechanical delay, with appropriate design of the SiC NEMS devices, it is possible to achieve ~1GHz operating frequency [15]. Also, active area can be considered as a less critical factor in terms of high temperature applications.

To further increase the reliability of the NEMS layer and reduce cost, we embed BIST circuitry in CMOS layer for detecting faults in NEMS circuits and replace certain units accordingly. Fig. 2 illustrates the BIST structure with a full adder as the example. To enhance reliability, we implement multiple copies of the full adder in NEMS layer. The CMOS BIST circuitry contains two parts: Pseudo Random Sequence Generator (PRSG) and an Output switching monitor. Like structures for traditional BIST [18], the PRSG is used to generate random sequences as testing input for the full adders. However, instead of using a signature analyzer, we implement an output switching monitor to analyze the output for reducing overhead. The output switching monitor contains an asynchronous counter for each output, which takes the output as its clock signal. The bit-widths of the counters are predefined according the expected number of switching with respect to the input sequence and the specific circuitry (full adder, in this case). Once enough number of switching is achieved for each output, the latch is set to be one. Finally if every output has enough switching, the circuit is considered as fault-free. Otherwise, the circuit is believed to have faults, and corresponding control signal (NoFault) is generated to select another copy of fault-free full adder. To balance the area overhead and detection accuracy, we insert BIST circuitry in a "moderate-grain", namely we choose proper size of logic as the unit of BIST insertion. For this specific example, the area overhead and thus power overhead of the CMOS BIST circuitry is about 1/10 of that of each NEMS full adder copy. Since we can use the BIST circuitry in a time-multiplexed way for a multi-bit adder, the overhead is reduced proportionally, such as 1/160 in a 16-bit ripple carry adder.

VII. CONCLUSION

We have presented a hybrid computing framework consisting of heterogeneous integration of two fundamentally dissimilar computing layers with complementary capabilities – a nanoelectronic and a nanomechanical computing layer – to

Table II: Comparison of power, critical delay and active area of NEMS switch and CMOS based ISCAS benchmarks

Circuit	Leakage Power		Dynamic Power		Critical Path delay		Active area	
	NEMS Circuit (pW)	CMOS Circuit (μW)	NEMS circuit (fJ/vec) 500ºC	CMOS FPGA (fJ/vec) 25ºC	NEMS circuit (μs) 500ºC	CMOS circuit (ns) 25ºC	NEMS Circuit (μm^2)	CMOS Circuit (μm^2)
c432	11.7	2.39	4.73E-13	1.27E-13	17.0	4.4	1014.4	21.08
c499	34.4	2.71	1.54E-12	3.84E-13	14.5	4.09	2976	61.42
c880	25.5	2.07	1.07E-12	2.92E-13	16.0	4.22	2304	48.82
c1908	32.4	2.37	1.60E-12	4.88E-13	19.0	5.29	2812.8	58.04
c2670	42.1	3.68	2.00E-12	5.04E-13	17.5	4.15	3993.6	81.94
c3540	65.6	6.03	2.20E-12	5.03E-13	23.0	6.48	6691.2	141.26
c5315	82.3	9.02	4.33E-12	1.28E-12	15.0	5.24	9785.6	202.83
c6288	160.0	14.8	4.74E-12	3.58E-12	52.0	13.17	15820.8	325.53
s298	4.74	2.96	5.06E-13	1.00E-13	5.00	1.5	969.6	19.96
s344	5.51	3.01	8.93E-13	8.36E-13	9.50	2.59	1062.4	22.09
s526	9.23	3.89	3.19E-12	9.34E-13	7.50	2.35	1465.6	30.35
s641	12.6	3.78	3.55E-12	9.28E-13	14.5	4.48	1392	28.29
s953	24.3	8.23	4.98E-12	1.09E-12	6.00	2.47	3232	67.11
s1196	32.6	8.60	1.51E-11	2.60E-12	9.00	3.5	3680	77.03
s1238	42.4	8.77	1.48E-11	2.64E-12	6.50	2.88	3664	76.19
s1423	60.1	13.7	7.28E-12	1.84E-12	30.0	8.92	5152	105.92
s5378	126.0	75.2	3.62E-11	9.46E-12	8.00	2.97	11849.6	241.76
s9234	93.5	28.7	2.21E-11	6.38E-12	16.5	3.53	9539.2	193.17

achieve high energy efficiency, programmability, and robustness of operation across wide operating range. It aims at merging the benefits of both layers while investigating and addressing the challenges with such heterogeneous system. The NEMS layer addresses the leakage and reconfigurability issues of nanoFET layer while allowing reliable operation at harsh environments. The nanoFET layer addresses the reliability and drivabiliy issues of the NEMS layer, while allowing high performance. Both device layers can benefit from choice of emerging materials (e.g. Graphene, silicon nanowires). We have fabricated a set of NEMS devices and validated the logic operation of some switches as well as logic gates. Based on the measured values of the switches, we have developed model for NEMS logic. Simulation results using this model appear very promising for harsh-environment operation using NEMS switches. We have also analyzed the complementary capabilities and symbiotic roles of the two layers. Effective integration of multiple layers can leverage emerging nanofabrication techniques, materials with superior electro-mechanical capabilities, and 3D integration technologies that address electro-thermal interaction between the layers.

ACKNOWLEDGEMENT

The authors acknowledge valuable inputs on the technical content from Dr. Philip Feng, Dr. Chris Zorman, Dr. Saibal Mukhopadhyay, Dr. Chris Papachristou and Dr. Muhannad Bakir.

REFERENCES

[1] P. Kogge et al., “Exascale computing study: technology challenges in achieving exascale systems”, DARPA Report, 2008.

[2] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. Thompson, and M. Christoph, “The changing automotive environment: high-temperature electronics”, IEEE Transactions on Electronics Packaging Manufacturing, vol. 27, no. 3, July 2004.

[3] J. Balfour, W.J. Dally, D. Black-Schaffer,V. Parikh, J.S. Park, “An Energy-Efficient Processor Architecture for Embedded Systems," Computer Architecture Letters, vol.7, no.1, pp.29-32, 2007.

[4] Y. Li et al, “Operating SOI CMOS technology in extreme environments,” Silicon Monolithic Integrated Circuits in RF Systems, 2003.

[5] P.G. Neudeck et al., “High-temperature electronics—A role for wide bandgap semiconductors”, Proc. of the IEEE, vol. 90, no. 6, June 2002.

[6] A.C. Patil et al., “Fully-monolithic, 600˚C differential amplifiers in 6H-SiC JFET IC technology,” Custom Integrated Circuits Conference, 2009.

[7] T.-H. Lee, S. Bhunia, and M. Mehregany, “Electromechanical Computing at 500°C with Silicon Carbide,” Science, vol. 329, no. 5997, pp. 1316-1318, Sep. 2010.

[8] H.F. Dadgour and K. Banerjee, “Design and analysis of hybrid NEMS-CMOS circuit for ultra low-power applications,” DAC, 2007.

[9] R. S. Chakraborty, S. Narasimhan and S. Bhunia, “Hybridization of CMOS with CNT-based nano electromechanical switch for low leakage and robust circuit design,” IEEE Trans. on Circuits and Systems, vol. 54, no. 7, pp. 2480-2488, Nov. 2007.

[10] K. Alzoubi et al., “Complementary nano-electromechanical switches for ultra-low power embedded processors”, GLSVLSI, 2009.

[11] F. Chen et al., “Integrated circuit design with NEM relays”, ICCAD, 2008.

[12] C. Chen et al, “Efficient FPGAs using nanoelectromechanical relays”, *FPGA*, 2010.

[13] X. Wang, S. Narasimhan, A. Krishna, F.G. Wolff, S. Rajgopal, T.-H. Lee, M. Mehregany, and S. Bhunia, “High-temperature (>500°C) FPGA using SiC nano-electro-mechanical system switches,” Design Automation and Test in Europe (DATE), 2011.

[14] S. Paul and S. Bhunia, "Computing with Nanoscale Memory: Model and Architecture," IEEE/ACM International Symposium on Nanoscale Architecture (NANOARCH), pp. 1-6, 2009.

[15] X.M.H. Huang, C.A. Zorman, M. Mehregany, and M.L. Roukes, “Microwave-frequency nanoelectromechanical systems,” Nature, vol. 421, pg. 496, 2003.

[16] M. Cho, C. Liu, D. H. Kim, S. Lim, and S. Mukhopadhyay, "Design Method and Test Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3D System," IEEE International Conference on Computer Aided Design (ICCAD), Nov. 2010.

[17] Process Integration, Devices and Structures, ITRS 2007 [Online] http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_PIDS.pdf

[18] M. L. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits," Boston, Springer, 2005.