Guest Editorial Computing in Emerging Technologies (First Issue)

AS THE scaling of CMOS technology is slowing down, device and technology community is actively exploring the potential alternatives to conventional CMOS transistors. The set of promising candidates beyond CMOS includes devices that operate using charge as the primary state variable like CMOS, but exhibits better electrostatics and/or transport properties. For example, tunneling field effect transistors (TFETs) exhibit ultralow leakage and sub-thermal switching slopes creating new opportunities in logic, memory, and analog/RF design. The devices based on complex oxides show interesting new properties. On the other hand, non-charge based post-CMOS devices such as memristors or spin-based devices possess fundamentally different operational behavior compared to conventional CMOS.

With the tremendous growth in the area of emerging technologies, it is critical to investigate the circuit, system, and computing approaches with these technologies to design a truly *beyond*-CMOS system. Such a *beyond-CMOS* systems may include post-CMOS devices, potentially integrated with CMOS electronics, and exploit advancements in heterogeneous packaging technologies. These complex beyond-CMOS systems will require innovative approaches in circuit, architecture, and system level design as well as associated modeling and design tools. To harness the true potential of the emerging nanoscale devices, innovative and unconventional computing models may be required.

This special issue focuses on circuit, architecture, and system aspects of computing in beyond-CMOS electronics. We received a large number of submissions (56) on circuit, architecture, and computing models in both charge and noncharge based emerging technologies. The papers were contributed by researchers from both academia and industry. Given the extremely large number of high-quality submissions that were received, it was decided to devote two consecutive JETCAS issues to the theme, in order to accommodate adequate number of high quality contributed papers. This issue, the first of two, features a total of 10 contributed articles selected through the highly competitive peer-review process.

The first five papers focus on exploiting the unique properties of two emerging technologies, namely, tunneling field-effect transistors (TFET) and memristors for design of logic, memory, analog circuits, and reconfigurable platforms.

The paper entitled "Design of Low Voltage Tunneling-FET Logic Circuits Considering Asymmetric Conduction Characteristics" by Moriris, *et al.* discusses the design strategies for low voltage logic gates using Heterojunction TFETs. In particular, the paper discusses the circuit characteristics, both favorable and unfavorable, arising due to the effect of asymmetric conduction in TFETs. The paper provides important guidelines for logic design using TFETs.

The paper entitled, "Evaluation of Stability, Performance of Ultra-Low Voltage MOSFET, TFET and Mixed TFET-MOSFET SRAM Cell with Write-Assist Circuits," by Chen *et al.* discusses static random access memory (SRAM) design using TFETs. Authors present a mixed TFET-MOSFET 8T SRAM cell that exploits both the merits of TFET and MOSFET devices and provide significant improvement in SRAM stability, ultra-low-voltage operation, and performance.

The paper entitled, "Tunnel FET RF Rectifier Design for Energy Harvesting Application," by Li, *et al.*, explores the analog/RF applications of Heterojunction TFETs. Authors show that steep-slope III-V Heterojunction TFET (HTFET) RF rectifiers have much higher power conversion efficiency over the Si FinFET. The capability of obtaining a high efficiency at a low RF input power range leads to the superiority of the HTFET RF rectifiers for battery-less energy harvesting applications.

The paper entitled "Memristive circuits for LDPC decoding," by Poikonen *et al.*, introduces efficient hybrid (CMOS-memristor) implementation of decoders in low-density parity check (LDPC) codes that exploits the properties of memristive circuits. Authors perform extensive circuit-level analysis to analyze decoder performance considering practical issues such as variance in memristance values and defects.

The paper entitled "Deign, Test and Repair of MLUT (Memristor Look-Up Table) Based Asynchronous Nanowire Reconfigurable Crossbar Architecture," by Choi *et al.* presents a "divide and conquer" based testing approach for efficiently locating defects in a memristor-based look up table (MLUT) that combines the benefits of memristive crossbar and asynchronous logic.

The final five papers explore the interactions of unique characteristics of emerging devices and nonconventional computing models to enable efficient beyond-CMOS systems.

The paper entitled, "Nontraditional Computation using Beyond-CMOS Tunneling Devices, by Sedighi *et al.*, investigates applications of tunneling devices for unconventional signal processing. The paper focuses on networks of interconnected nonlinear elements that can process data coming from a large number of sensors in an analog fashion. It shows that tunneling devices can lead to reduced complexity and/or enhanced power efficiency of such platform.

The paper entitled "Exploiting Synchronization Properties of Correlated Electron Devices in a Non-Boolean Computing Fabric for Template Matching," by Parihar *et al.* studies application of post-CMOS technologies to non-Boolean computing

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platform. The paper investigates coupled and scalable relaxation-oscillators utilizing the metal–insulator–metal transition of vanadium-dioxide (VO2) thin films and demonstrates the potential use of such a system in a non-Boolean computing paradigm.

The paper entitled "A Non-Volatile Associative Memory-Based Context-Driven Search Engine Using 90 nm CMOS/MTJ-Hybrid Logic-in-Memory Architecture," by Jarollahi presents algorithm, architecture, and fabrication results of a nonvolatile context-driven search engine. The fabricated chip demonstrates successful integration of CMOS and magnetic tunneling junction (MTJ). The measurement results demonstrate significant improvement in energy and performance compared to a conventional content-addressable memory (CAM) based design.

The paper entitled "Energy-efficiency and Accuracy of stochastic Computing Circuits in Emerging Technologies," by Moons *et al.* assesses the feasibility and effectiveness of stochastic computing (SC) in emerging technologies. It discusses energy and accuracy considerations in SC based systems.

The paper entitled "Biconditional Binary Decision Diagrams: A Novel Canonical Logic Representation Form," by Amaru *et al.* introduces a novel Biconditional Binary Decision Diagram (BBDD) structure, which can provide highly compact representation of Boolean function and is particularly attractive for technologies that use comparator as circuit primitive. Authors validate major benefits of BDDD in circuit representation for both nanoscale CMOS and emerging technologies.

We hope that the readers will enjoy the selected papers and that this issue will serve as a stimulus for opening up new research in the area of computing in emerging technologies. We would like to express our sincere appreciation to authors of all the papers submitted to this special issue. The quality of the submissions was excellent in general and selecting a subset of the papers for publication was a major challenge. We sincerely thank the reviewers for delivering high-quality reviews in a timely manner that helped us address this challenge and improve the quality of the accepted papers. We would also like to express our gratitude to Prof. Manuel Delgado-Restituto, IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (JETCAS) Editor-in-Chief, and Prof. Yen-Kuang Chen, the Deputy-Editor-in-Chief, and the editorial team of JETCAS for their constant support without which this special issue would not have been possible. We would like to conclude by reminding all the interested people that a second JETCAS issue devoted to "Computing in Emerging Technologies" will be published in the next quarter. It will feature several high-quality contributed papers and a perspective paper from the guest editors.

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