

Guest Editorial

Computing in Emerging Technologies (Second Issue)

IN THE quest of a potential alternative to CMOS at the end of its roadmap, multitude of research efforts have been directed towards investigating novel devices with unique characteristics. These emerging devices hold tremendous potential in achieving higher integration density (in the order of 10^{10} devices/cm²), higher performance, and increased energy efficiency for computation. On the other hand, these devices also brings in interesting challenges to logic design, for example, difficulty to construct a cascaded irregular logic structure. The dense and periodic structures as well as bi-stable nature of many nanodevices make them amenable to large high-density memory array design. Moreover, self-assembly of many nanostructures is efficient for a bottom-up system design flow, thus making them suitable for building reconfigurable computing paradigms.

These tectonic shifts in device technology impact the design and test of integrated systems in profound ways. Transforming these nanodevices into nanocomputing framework may require nontraditional computing model as well as circuit/architecture level design approaches. Along with using nanodevices as “better switches” in existing “switch based” implementations of logic functions, it is equally important to explore different approaches to fully exploit the benefits of nanodevices while mitigating some of the major shortcomings, such as high defect rate and lack of gain. Since many nanodevices need to be interfaced with CMOS switches, a well-designed nanoscale memory structure needs to substantially reduce the CMOS overhead per memory cell. Moreover, memory structures realized using nanodevices should have very well-defined CMOS interfaces to facilitate CMOS-nano hybridization. A reconfigurable computing architecture is promising for many devices since it facilitates mapping arbitrary applications in a generic periodic fabric using bottom-up manufacturing. Furthermore, a transition into the beyond-CMOS era is expected to drive large shift in the design of secure systems. First, the properties of emerging nanoscale devices (e.g., large variations, power/timing asymmetry, and non-volatility) could lead to new attack modalities. Second, new defense mechanisms (e.g., new design for security primitives) may be enabled by the unique characteristics of nanoscale devices.

This special issue focuses on circuit, architecture, and system aspects of computing in beyond-CMOS electronics. We received a large number of submissions (56) on circuit, architecture, and computing models for both charge and noncharge based emerging technologies. The papers were contributed by researchers from both academia as well as industry. Given the extremely large number of high-quality submissions that were

received, it was decided to devote two consecutive JETCAS issues to the theme, in order to accommodate adequate number of contributed papers. All submitted papers went through one round of rigorous peer review process. A selected subset of papers received at least one iteration of revision and review before being accepted. Approximately 33% of the papers are accepted and distributed between the two special issues. This issue, the second of two, features a total of 10 contributed papers selected through the highly competitive peer-review process discussed before. It also features a perspective paper from the guest editors on device-circuit-architecture level design using promising spin-based devices.

The first two papers focus on computing with spin. The tutorial paper titled “Exploring Spin Transfer Torque Devices for Unconventional Computing” by the guest editors highlights the changing paradigm of computing in post-CMOS technology regime with a case study. It considers system design with spintronic devices that use the spin of electrons as state variable. These devices exhibit promising characteristics in terms of both information processing as well as nonvolatile storage. The paper reviews several spintronic devices, which allow manipulation of device state by current-induced spin transfer torque. Next, it presents efficient unconventional computing fabrics with these devices including neuromorphic computing and in-memory reconfigurable computing.

Cascading logic gates is a critical challenge for the development of spintronic logic circuits. The paper entitled, “Emitter-Coupled Spin-Transistor Logic: Cascaded Spintronic Computing Beyond 10 GHz,” by Sahakian *et al.*, presents a logic family exploiting magnetoresistive bipolar spin-transistors to achieve a complete spintronic logic family with feasibility of cascading gates. This logic family, emitter-coupled spin-transistor logic, inspires a pathway for high-performance spintronic computing beyond 10 GHz.

The following four papers discuss design opportunities using emerging memory technologies. Spin transfer torque magnetic random access memory (STT-MRAM) is an attractive emerging memory technology with desirable characteristics like nonvolatility, high access speed, and low operational power. However, transient and permanent failures in STT-RAM remain a major hurdle, specifically at scaled dimensions. The paper entitled “Yield and Reliability Improvement Techniques for Emerging Nonvolatile STT-MRAM,” by Zhao *et al.*, discusses a synergistic framework, named sECC, which integrates both the Error Correction Coding and Fault-Masking techniques to address simultaneously the permanent and transient faults.

The paper entitled “Domain Wall Magnets for Embedded Memory and Hardware Security,” Iyengar *et al.*, focuses on an

emerging nonvolatile memory, namely domain wall memory (DWM), which is a promising candidate for next-generation cache due to its excellent density, standby power, and retention capabilities. It presents a physics-based model of DWM that helps characterize the process variations as well as joule heating effects. Next, it shows that the effect of process variations can be leveraged for device authentication by building robust security primitives, namely, physical unclonable functions.

The paper entitled “Phase Change Memory Write Cost Minimization by Data Encoding,” by Mirhoseini *et al.*, deals with phase change memory (PCM), which is viewed as a promising nonvolatile memory in the sub-10nm technology regime. The paper targets optimizing PCM's write performance through judicious encoding of data that exploits the asymmetries in PCM read/write operations. The proposed solution applies to any single or multi-level cell PCM as well as other asymmetric memories. The paper demonstrates the efficacy of the encoding approach and reports the hardware overhead.

Redox-based resistive switching devices (ReRAM) form an emerging class of nonvolatile storage elements suited for nanoscale memory applications. The paper entitled “A Complementary Resistive Switch-based Crossbar Array Adder,” by Siemon *et al.*, introduces the concept of complementary resistive switches (CRS) for passive crossbar arrays using CRSs. This paper discusses two multi-bit adder schemes using the CRS-based logic-in-memory approach.

The following three papers discuss system level challenges and opportunities. The paper entitled “A Fast System-Level Design Methodology for Heterogeneous Multi-core Processors Using Emerging Technologies,” by Pan *et al.*, presents a system-level design framework for early-phase evaluation and optimization of processors designed with post-CMOS technologies. It considers appropriate models for performance, memory subsystem and interconnects and allows optimizing chip throughput for a specific device technology and processor architecture family under power, thermal and area constraints. For various technology and architecture choices, the paper provides the best design trade-offs that can be obtained using the proposed framework.

The paper entitled “Multi-Level Mapping of Nanocomputer Architectures Based on Hardware Reuse,” by Yakymets *et al.* tackles the problem of mapping large applications to hierarchical architectures built with emerging nanoscale devices. It presents a “O-cycle” design flow that combines the concepts of intellectual property reuse and multi-level mapping. The resultant mapping framework becomes scalable and efficient in terms of circuit design time. It also enables effective optimization of power, critical path delay and die area. The paper demonstrates significant improvement in power and delay for common circuit topologies.

The paper entitled “Reconfiguration-Based VLSI Design for Security,” by Liu *et al.* presents secure nanoelectronic system design approaches by exploiting the nature of reconfigurable computing paradigm. It shows that a reconfigurable imple-

mentation of a logic function effectively obfuscates it, thus making it difficult for an adversary to reverse-engineer the design. Additionally, ability to dynamically reconfigure a logic function makes it more secure through the concept of moving target defense. The paper also presents a reconfigurable reversible computing-based cryptography approach and a general design-for-security solution that exploits reconfiguration. The approaches are validated with case studies using a SPARC V8 LEON2 processor.

The special issue presented several papers that leverages the unique characteristics of emerging technologies for circuit and system level design. However, the need for significant effort in developing circuit simulation framework for new devices is a major challenge for progress in this field. The paper entitled, “Advances in Computational Modeling of Electronic Devices based on Graphene,” by Vargas-Bernal presents the computational modeling methodologies to address this important challenge, focused mainly on graphene based devices.

We hope that the readers will enjoy the selected papers and that this issue will serve as a stimulus for opening up new research in the area of computing in emerging technologies. We would like to express our sincere appreciation to authors of all the papers submitted to this special issue. The quality of the submissions was excellent in general and selecting a subset of the papers for publication was a major challenge. We sincerely thank the reviewers for delivering high-quality reviews in a timely manner that helped us address this challenge and improve the quality of the accepted papers. We would also like to express our gratitude to Prof. Manuel Delgado-Restituto, JETCAS Editor-in-Chief, and Prof. Yen-Kuang Chen, the Deputy-Editor-in-Chief, and the editorial team of JETCAS for their constant support without which this special issue would not have been possible.

SAIBAL MUKHOPADHYAY, *Guest Editor*
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA 30332 USA

SWARUP BHUNIA, *Guest Editor*
Electrical Engineering and Computer Science Department
Case Western Reserve University
Cleveland, OH 44106 USA

HILLERY C. HUNTER, *Guest Editor*
Computer Architecture Department
IBM T. J. Watson Research Center
Yorktown Heights, NY 10598 USA

KAUSHIK ROY, *Guest Editor*
Electrical and Computer Engineering Faculty
Purdue University
West Lafayette, IN 47907 USA



Saibal Mukhopadhyay (S'99–M'07–SM'11) received the B.E. degree in electronics and telecommunication engineering from Jadavpur University, Kolkata, India, and the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, USA, in 2000 and 2006, respectively.

He was a Research Staff Member at IBM T. J. Watson Research Center from September 2006 to September 2007. He is currently an Associate Professor with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA. His current research interests include low-power and robust circuits in emerging technologies, low-voltage power converters and integrated voltage regulators, low-power mixed-signal systems, 3-D integration, and energy-efficient neural computing. He has authored or co-authored over 125 papers in refereed journals and conferences, and holds five U.S. patents.

Dr. Mukhopadhyay was a recipient of the Office of Naval Research Young Investigator Award in 2012, the National Science Foundation CAREER Award in 2011, the IBM Faculty Partnership Award in 2009 and 2010, the SRC Inventor Recognition Award in 2008, the SRC Technical Excellence Award in 2005, the IBM Ph.D. Fellowship Award for years 2004 to 2005. He has received Best Paper Awards in IEEE TRANSACTIONS ON COMPONENTS, MANUFACTURING AND PACKAGING TECHNOLOGY (2014), IEEE Transaction on VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (2014), IEEE/ACM International Low-power Electronics and Design (2014), and IEEE International Conference on Computer Design (2004). He has served as Program Co-chair in International Symposium on Quality Electronic Design (ISQED), 2015 and in the technical program committee of major IEEE and ACM conferences.



Swarup Bhunia (SM'14) received the B.E. (Hons.) degree from Jadavpur University, Kolkata, India, and the M.Tech. degree from the Indian Institute of Technology (IIT), Kharagpur, India. He received the Ph.D. degree from Purdue University, West Lafayette, IN, USA, in 2005.

Currently, he is T. and A. Schroeder Associate Professor of Electrical Engineering and Computer Science at Case Western Reserve University, Cleveland, OH, USA. He has over 10 years of research and development experience with over 150 publications in peer-reviewed journals and premier conferences. His research interests include low-power and robust design, hardware security and trust, adaptive nanocomputing and novel test methodologies. He has been serving as an Associate Editor of the ACM *Journal of Emerging Technologies in Computing Systems*.

Dr. Bhunia received IBM Faculty Award (2013), National Science Foundation (NSF) career development award (2011), Semiconductor Research Corporation (SRC) Inventor Recognition Award (2009), and SRC technical excellence award (2005), and several best paper awards/nominations. He has been serving as an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS and as a Guest Editor of the IEEE DESIGN & TEST OF COMPUTERS (2010, 2013). He has served as Program Chair for NANOARCH 2013, International Symposium on VLSI Design and Test (VDAT), 2014 and in the technical program committee of major IEEE and ACM conferences.



Hillery C. Hunter received the Ph.D. degree in electrical engineering from the University of Illinois, Urbana-Champaign, IL, USA.

She is currently the Research Memory Strategist and Senior Manager of the Computer Architecture Department at IBM's T. J. Watson Research Center, Yorktown Heights, NY, USA. She is interested in cross-disciplinary technology topics, spanning silicon to system architecture to achieve new solutions to traditional problems. She has most recently published in the areas of DRAM main memory systems and embedded DRAM, and gained development experience serving as IBM's server and mainframe DDR3-generation end-to-end memory power lead.

Dr. Hunter was selected by the National Academy of Engineering for its Frontiers in Engineering Symposium, a recognition as one of the top young engineers in America, in 2010. She is a member of the IBM Academy of Technology.



Kaushik Roy (F'12) received the B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and the Ph.D. degree from the Electrical and Computer Engineering Department, University of Illinois, Urbana-Champaign, IL, USA, in 1990.

He was with the Semiconductor Process and Design Center of Texas Instruments, Dallas, TX, USA, where he worked on FPGA architecture development and low-power circuit design. He joined the Electrical and Computer Engineering Faculty at Purdue University, West Lafayette, IN, USA, in 1993, where he is currently Edward G. Tiedemann Jr. Distinguished Professor. His research interests include spintronics, device-circuit co-design for nanoscale Silicon and non-Silicon technologies, low-power electronics for portable computing and wireless communications, and new computing models enabled by emerging technologies. He has published more than 600 papers in refereed journals and conferences, holds 15 patents, graduated 60 Ph.D. degree students, and is co-author of two books on low power CMOS VLSI design (Wiley and McGraw Hill).

Dr. Roy received the NSF Career Development Award in 1995, IBM faculty partnership award, ATT/Lucent Foundation award, 2005 SRC Technical Excellence Award, SRC Inventors Award, Purdue College of Engineering Research Excellence Award, Humboldt Research Award in 2010, 2010 IEEE Circuits and Systems Society Technical Achievement Award, Distinguished Alumnus Award from Indian Institute of Technology (IIT), Kharagpur, Fulbright-Nehru Distinguished Chair, DoD National Security Science and Engineering Faculty Fellow (2014–2019), and several best paper awards. He was a Purdue University Faculty Scholar (1998–2003). He was a Research Visionary Board Member of Motorola Labs (2002) and held the M. K. Gandhi Distinguished Visiting faculty at Indian Institute of Technology (Bombay). He has been in the editorial board of IEEE DESIGN & TEST, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and IEEE TRANSACTIONS ON ELECTRON DEVICES.