

NANOMANUFACTURING OF SiC CIRCUITS — NANOMECHANICAL LOGIC AND NEMS-JFET INTEGRATION

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ABSTRACT

Silicon carbide (SiC) remains the most promising semiconductor for developing harsh environment microsystems, particularly in applications where temperatures exceed 300 °C. While significant progress has been made in the development of more conventional junction field effect transistors (JFET), many challenges remain, particularly in the realization of robust digital logic circuits. The authors have been developing SiC-based electromechanical switches towards digital logic circuits, the goal being hybrid integration, with high performance JFET electronics complementing ultralow power logic enabled by nanoelectromechanical systems (NEMS). In this paper, the advances made in NEMS logic technology are first discussed. Areas that require additional research are detailed. A simplified integration scheme is proposed.

KEYWORDS: Silicon Carbide, NEMS, JFET, Hybrid Integration, High Temperature, Harsh Environment

INTRODUCTION

Sensors and circuits capable of operating in harsh environments characterized by high temperature (300-700 °C) and/or high radiation (1-30 Mrad) are highly desirable in areas such as aircraft engines, oil refining and exploration, chemical/nuclear plants, geothermal logging, and space exploration. In addition, the high junction temperatures and consequently expensive thermal management and heat sinking requirements of conventional CMOS electronics have led to increased interest in alternative high-temperature-capable circuit technologies.

Conventional Si metal-oxide-semiconductor field-effect transistor (MOSFET) technology is limited to 300 °C even when implemented with the silicon-on-insulator (SOI) approach [1]. This is because at elevated temperatures, electrical conductivity becomes undesirably influenced by intrinsic carriers instead of the designed doping. Intrinsic carriers in turn affect p-n junction leakage. Temperature also affects thermionic leakage (limited by the semiconductor bandgap). Finally, mobility and velocity saturation effect degrade with temperature. The aforementioned issues lead to, amongst other things, a reduction in drain current and threshold voltage with temperature in conventional MOSFET devices [1].

SiC is a promising semiconductor for hostile environment microsystems because of its excellent physical and electrical properties, including wide bandgap, high thermal conductivity, mechanical strength, chemical stability, high electric field breakdown, and relatively high carrier saturation velocity [2]. Wide bandgap (~3-eV) semiconductors have much lower intrinsic carrier concentrations than Si and thus are not affected by intrinsic carrier conductivity issues or leakage currents until beyond 600 °C. The wide bandgap also makes fabricated electronics rad hard, giving it a higher tolerance to soft errors induced by high-energy particles. SiC is chemically inert and is not susceptible to thermally driven impurity diffusions at the targeted operating temperature range. The material is also available in bulk wafer form.

Our team and researchers from NASA have successfully demonstrated SiC-based sensors and JFET electronics at temperatures beyond 550 °C [3]. However, several issues make realization of robust digital logic circuits based on SiC JFET challenging. These include large transistor size, high threshold voltage and low switching speed. Leakage current also increases significantly at elevated temperatures. Finally, multi-level cascaded logic realization using depletion-mode negative threshold devices poses a major challenge.

NEMS switches offer an attractive alternative to realizing low-power, high-performance logic circuits. The on-off transitions of these switches can be controlled by electrostatic actuation and the physical air/vacuum gap results in minimal off-state leakage. Thus extremely high I_{ON}/I_{OFF} ratio can be achieved even at elevated temperatures. In addition, the devices possess the operating speed, power and footprint comparable to conventional MOSFET. NEMS switches however, do not naturally provide the typical voltage/current gain observed in transistors. This affects drivability and hence realization of cascaded logic circuits. Hybrid integration of SiC NEMS with SiC JFET-based circuits is a potential solution to this issue. This appears feasible given that the SiC NEMS logic technology is naturally compatible with our SiC JFET-based integrated circuit technology. Such a platform technology has the potential to provide new opportunities for high temperature mixed-signal electronics, while also being able to address the high leakage power issue in JFET devices at high temperatures.

The ideal NEMS-JFET hybrid technology platform imposes challenges to be addressed at the device, circuit and architecture levels. In this paper we limit our discussions to integration concerns at the device level. We begin with a review of our current results in NEMS switches and logic design. Modifications of the basic switch designs are presented for implementation in more elaborate building blocks like complex data path, e.g., arithmetic logic unit (ALU). Issues such as contact resistance and failure mechanisms observed during testing are described along with potential techniques to mitigate them. We conclude by briefly presenting a designed process for monolithically integrating a NEMS with a JFET.

SiC NEMS SWITCH DESIGN

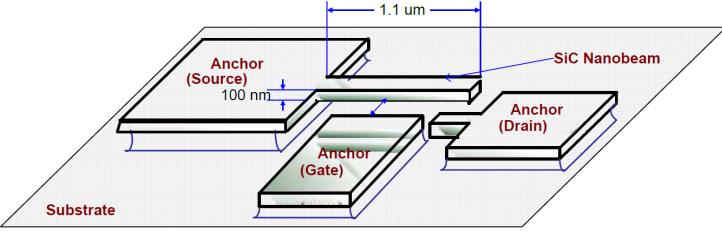


Figure 1: Schematic illustration of the poly-SiC 3-terminal NEMS switch. The various dimensions are not to scale. Movement of cantilever due to electrostatic attraction between source and gate causes the beam to contact drain.

where k is the stiffness of the beam, L , w , and t are the length, width and thickness of the beam respectively, g_o is the initial gap, ε_0 is the permittivity of free space, A is the overlap area and E is the Young's modulus of the beam material (SiC). The switching time may be written as [4],

$$t_s \approx \sqrt{27/2} (V_{on}/\omega_o V_{act}) \propto (L^2/w)(V_{on}/V_{act})\sqrt{\rho/E} \quad (2)$$

where ω_o is the stiffness of the beam, V_{act} is the applied actuation voltage and ρ is the density of SiC. Clearly there exists a trade-off between threshold voltage and operating frequency of the NEMS switch. However, by moving to nanoscale dimensions and leveraging novel beam/switch structures, it is possible to realize switches with low turn-on voltages ($\leq 3V$) and fast switching times ($\leq 1\mu s$ or well in the $<100ns$ regime).

A scanning electron microscope (SEM) image of a poly-SiC 3-T lateral switch is shown in Fig. 2. The device was patterned using electron-beam lithography and etched by DRIE using a 40 nm-thick Ni mask. Release was accomplished in a critical-point dryer. For a similar 8 μm long, 150 nm wide switch with a 120 nm gap, the operating voltage was measured to be ~ 4.70 V. Reliable operation was demonstrated for 21+ billion cycles at 25 °C and 2+ billion cycles at 500 °C [5].

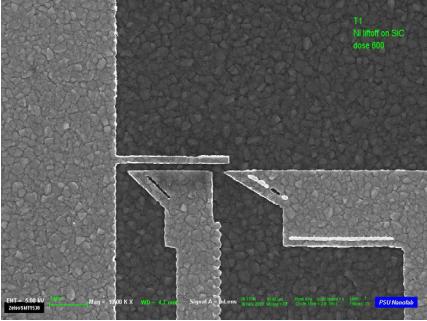


Figure 2: Fabricated 3-T poly-SiC switch and its close-up view. Beam dimensions: length, 3 μm ; width, 200 nm; and switching gap, 150 nm.

The basic 3-terminal (3-T) NEMS switch with terminals corresponding to gate (G), source (S) and drain (D) is shown in Fig. 1. The switch is electrostatically actuated laterally (in-plane) and is realized from doped ($N_D \sim 1 \times 10^{20} \text{ cm}^{-3}$) polycrystalline silicon carbide (poly-SiC). The sacrificial layer technique is used as the fabrication approach. Key design considerations include appropriate choice of dimensions together with doping levels of the JFET for achieving compatible threshold voltage as well as device scaling. Based on lumped parameter models, the equation for the switch-on voltage V_{on} may be written as [4],

$$V_{on} \approx (8kg_o^3/27\varepsilon_0 A)^{1/2} \propto \sqrt{Ew^3g_o^3/L^2} \quad (1)$$

In the 3-T switch design, the electrostatic force will pull the beam towards the drain irrespective of the polarity of the voltage difference between gate and the source. Thus the design can be used as a pull-up (PMOS) or pull-down (NMOS) switch by connecting the source terminal to V_{DD} or V_{SS} . Figure 3a and 3b are SEMs of a fabricated inverter. In [6] we reported successful operation of an inverter at 500°C in air with $V_{DD}=6V$ and $V_{SS}=-6V$, at an operating speed of 500 kHz. The design and fabrication process mirror that of the 3-T switch. A complementary logic style is implemented to reduce noise sensitivity and enable low static-power consumption. The two beams are dimensionally identical with length, width and actuation gap corresponding to 8 μm , 200 nm and 150 nm, respectively. The logic level (Fig. 3c) is higher than that in existing Si logic devices, which operate at 3V or lower. However, the threshold voltage of the fabricated switches is compatible to other competing high-temperature electronics [7]. The active area of the demonstrated inverter is $\sim 8 \mu m^2$, about three orders of magnitude smaller than most reported high-temperature, JFET-based logic gates, which have gate lengths ranging from tens to few hundreds of microns [7]. The measured leakage current in the off-state is less than 10 fA.

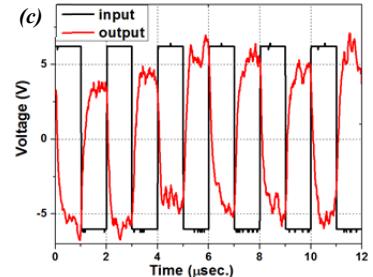
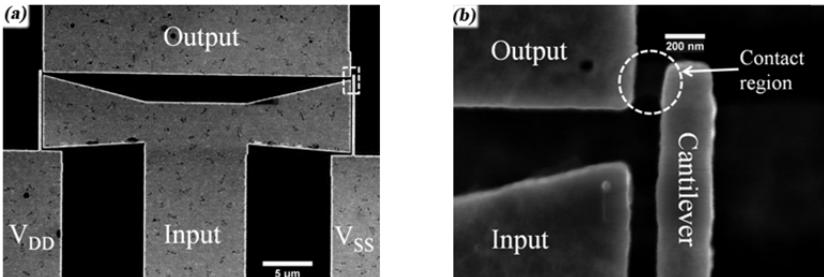


Figure 3: SEM images of the poly-SiC NEMS inverter. (a) Top view, (b) Close-up view, and (c) Measured input/output waveform at 500 °C [6].

When implementing more complex circuits like an ALU, it is preferable to minimize the number of active elements (actuating beams) for improvements in performance and robustness as well as reduction in device area. Figures 4a and 4b show conceptual drawings of a 4-T and 7-T switch respectively, using multilayer beams with separate control and S/D terminals. With respect to Fig. 4a, the cantilever is made of insulating poly-SiC or silicon nitride. The two conducting segments on the sidewall of the beam are made of doped SiC and electrically isolated from each other. When the voltage between G and B, $V_{GB} \geq V_{on}$, the beam moves towards G and forms a connection between S and D. By connecting B to V_{SS} or V_{DD} , we get a PMOS or NMOS pass transistor-like cell. The 7-T switch operates similar to the 4-T one.

The connection in Fig. 4b makes the 7-T switch act like a 2x1 MUX. Since in digital logic, the G voltage can only be logic low or high, the cantilever gets pulled in towards one side only. The corresponding S value will get transmitted to D, which realizes the function of a MUX.

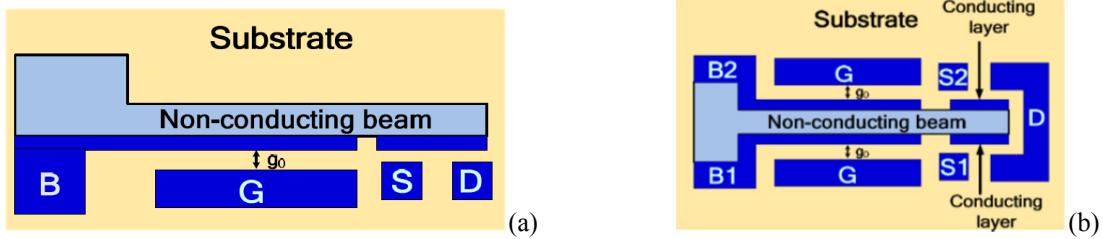


Figure 4: Designs of multiple-terminal NEMS switches for logic. (a) 4-T multi-layer beam switch, and (b) 7-T multi-layer switch, for efficient implementation of 2x1 multiplexer.

SWITCH RELIABILITY IMPROVEMENT

Failure mechanisms we have so far observed include the following: (1) Stiction, with the beam touching both drain/gate (Fig. 5a); (2) Mechanical fracture near the anchor of the beam; (3) Incomplete pattern delineation at the e-beam lithography process step or due to material re-deposition in the actuation gap during etching of the device layer, a result of aggressive feature scaling (Fig. 5b); (4) Cantilever deflection caused by localized stress leading to higher than designed actuation voltages or no actuation at all (Fig. 5c).

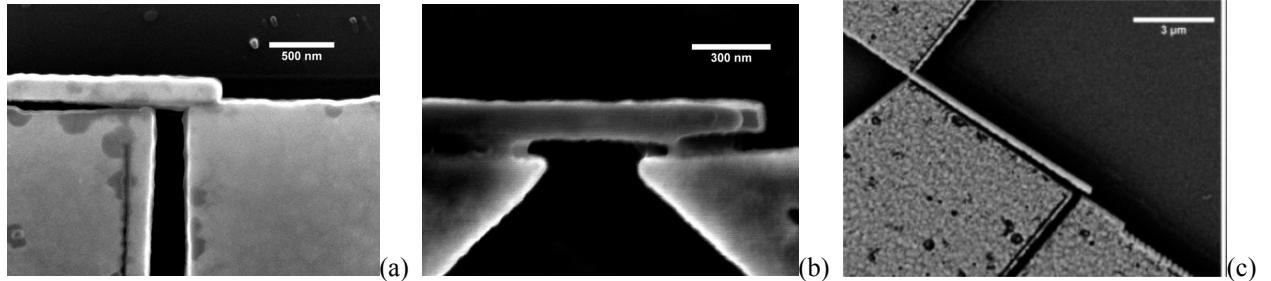


Figure 5: Typical switch failure mechanisms observed in our experiments. (a) Stiction with beam touching drain and gate, (b) Incomplete delineation of beam during lithography/etching, and (c) Effects of stress in device layer.

Process-based approaches to mitigating these issues include: (1) optimizing process conditions of the film deposition step for appropriate stress and stress gradient, (2) polishing the poly-SiC film for improved feature resolution during patterning and etching, (3) optimization of the e-beam lithography step to reduce trade-off between resolution and edge roughness and (4) optimization of the etch process to reduce etch lag and re-deposition.

Design-based approaches include varying beam cross-section near the base or a curved beam design. The drain contact may also be positioned closer to the beam than the gate. Other options include tapering the gate electrode or replacing the cantilever design with a doubly-clamped beam and repositioning of the gate and drain to mitigate simultaneous contact while also reducing actuation voltage.

SWITCH CONDUCTANCE IMPROVEMENT

In the poly-SiC NEMS devices we have fabricated and tested, the contact resistances are often in the $M\Omega$ ranges. The contact resistances of the switches are generally dominated at low actuation voltages by the native oxide formed on the switch contacting surfaces. At higher applied voltages, the calculated contact resistance values using Sharvin's model fit the measured values well [5]. To improve its conductivity, graphitized SiC surface is an attractive solution since the electrical conductivity of the resultant graphite/graphene surface is exceptional. The requisite processing does not alter the key dimensions of the device given that only a few atomic layers of materials are affected. However, conducting the experiment under UHV and at a temperature $> 1200^\circ C$ requires an expensive vacuum chamber, pumping system, and heating tool. We have attempted an alternative approach – graphitize the SiC surface by using laser energy. We have gathered some

interesting and encouraging preliminary results based on this attempt [5]. We believe this could possibly lead to a highly innovative approach toward new generations of high-performance SiC NEMS switches.

Our graphitization process involves XeCl laser treatment of the SiC surface, to convert the SiC surface into a carbon-rich, more conductive layer. Subsequent TEM and XPS studies indicate that a few to 10nm-thick nanographite ribbon structure has been obtained, repeatedly, from such a process. The measured resistivity of such surface layers is as low as $0.004 \Omega\cdot\text{cm}$.

HYBRID INTEGRATION OF SiC NEMS WITH SiC JFET

A NEMS-last approach is envisioned. The hybrid implementation may be achieved by modifying and extending the SiC JFET fabrication process. A possible integration solution, shown in Fig. 6, consists of separate layers for the JFET and NEMS logic, with necessary interconnect layers between the two device layers. The poly-SiC required for the NEMS switches is deposited at 900°C , determined by our current LPCVD process technology. These temperatures are not a concern as diffusion in SiC even at these temperatures is negligible. The JFET process flow remains the same till the step of creating access to the contact metal. Prior to doing so, a poly-SiC thin film is deposited to the desired thickness on the silicon dioxide passivation layer. The poly-SiC film is then patterned (Fig. 6a). Contact metal is then deposited and patterned on the NEMS. Finally, the oxide beneath the NEMS switches and vias to the JFET are opened in hydrofluoric acid.

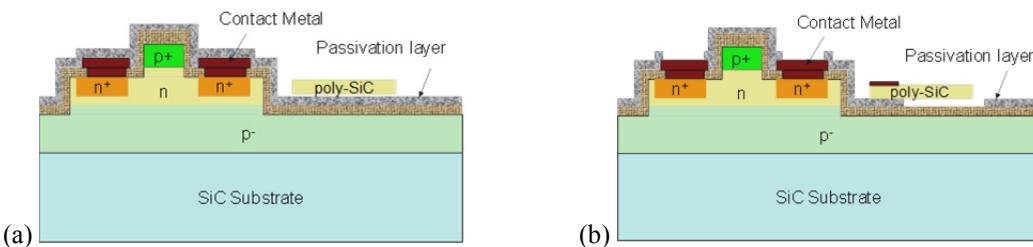


Figure 6: Process flow for NEMS-JFET hybrid integration. (a) Deposition and patterning of poly-SiC, (b) Release of NEMS structures.

CONCLUSION

NEMS logic is emerging as a complementary technology path towards realizing ultralow power harsh-environment-capable circuits using SiC. We have successfully demonstrated electromechanical operation of 3-terminal switches and a basic logic gate, an inverter, at temperatures up to 500°C , as well as very low voltage ($V_{\text{on}} \sim 1\text{V}$) SiC NEMS logic switches employing lithographically patterned, very thin SiC nanowires. Two major concerns including reliability and conductance at the device level have been discussed. A simplified integration process has been discussed that leverages the wide bandgap properties of SiC. Significant challenges remain, not only at the device level, but also at the circuit and architecture level. Reliability and contact conductance issues together with the demonstration of additional logic gates like NAND and XOR remain as the challenging topics for our ongoing and future explorations.

ACKNOWLEDGEMENTS

This work is supported by Defense Advanced Research Projects Agency (DARPA) under grants N66001-07-12031, NBCH2050002 and National Science Foundation (NSF) under grant #1116102. We would like to thank Drs. Ryan Lu, Chris Huynh, Ayax Ramirez, and Steve Russell at the SPAWAR, San Diego, CA, for assistance with the SiC graphitization.

REFERENCES

- [1] P. G. Neudeck, R. S. Okojie, L.-Y. Chen, "High-Temperature Electronics – A Role for Wide Bandgap Semiconductors?" *Proc. IEEE*, vol. 90, pp. 1065-1076, 2002.
- [2] P. G. Neudeck, "SiC Technology," in *The VLSI Handbook*, 2nd Ed., W.-K. Chen, Ed., Boca Raton, Florida: CRC Press, pp. 5.1-5.34, 2007.
- [3] P. G. Neudeck, S. L. Garverick, D. J. Spry, L.-Y. Chen, G. M. Beheim, M. J. Krasowski, M. Mehregany, "Extreme Temperature 6H-SiC JFET Integrated Circuit Technology," *Physica Status Solidi A*, vol. 206, pp. 2329-2345, 2009.
- [4] X. L. Feng, M. H. Matheny, C. A. Zorman, M. Mehregany, M. L. Roukes, "Low Voltage Nanoelectromechanical Switches Based on Silicon Carbide Nanowires," *Nano Letters*, vol. 10, pp. 2891-2896, 2010.
- [5] T.-H. Lee, *Ph.D. Dissertation*, Case Western Reserve University, Cleveland, Ohio, 2010.
- [6] T.-H. Lee, S. Bhunia, M. Mehregany, "Electromechanical Computing at 500°C with Silicon Carbide," *Science*, vol. 329, pp. 1316-1318, 2010.
- [7] A. C. Patil, X.-A. Fu, C. Anupongpongarch, M. Mehregany, S. L. Garverick, "6H-SiC JFETs for 450°C Differential Sensing Applications," *J. Microelectromech. Syst.*, vol. 18, pp. 950-961, 2009.

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