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Low Power Design Under Parameter Variations

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Abstract

Design considerations for low-power operations and robustness with respect to variations typically impose contradictory design requirements. Low-power design techniques such as voltage scaling, dual-V_{th} and gate sizing can have large negative impact on parametric yield under process variations. In this tutorial, we focus on circuit/architectural design techniques for low power under parameter variations. We consider both logic and memory design and encompass modeling, analysis as well as design methodology to simultaneously achieve low power and variation tolerance. Design techniques to minimize power under parametric yield constraint as well as major process adaptation techniques using voltage scaling, adaptive body biasing or logic restructuring will be presented. Techniques to deal with within-die parameter variations in logic and memory circuits primarily caused by random dopant fluctuations will be discussed with emphasis on frequency assignments and body biasing. Finally, we will discuss temperature-aware design, dynamic adaptation to temperature and cover on-going research activities in related area such as low-power and variation tolerant multi-core processor design.

Categories & Subject Descriptors: B.6.1 Design Styles, B.6.3 Design Aids, B.7.1 Types and Design Styles, B.3.1 Semiconductor Memories.

General Terms: Design, Algorithm, Performance.

Keywords: Low Power Design, Process Variations

Bio

Swarup Bhunia is currently an assistant professor of Electrical Engineering and Computer Science at Case Western Reserve University. He received his Ph.D. from Purdue University, IN, USA, in 2005. He has worked in the semiconductor industry on RTL synthesis, verification, and low power design for about three years. His research interest includes low power electronics, variation tolerance, adaptive computing and novel test methodologies. He has received SRC technical excellence award (2005), Best paper award in International Conference on Computer Design (ICCD 2004), Best paper award in Latin American Test Workshop (LATW 2003), and Best paper nomination in Asia and South Pacific Design Automation Conference (ASP-DAC 2006).

Kaushik Roy is currently a Professor and holds the Roscoe H. George Chair of Electrical & Computer Engineering at Purdue University, IN, USA. He received his Ph.D. degree from the electrical and computer engineering department of the University of Illinois at Urbana-Champaign in 1990. His research interests include VLSI design/CAD for nanoscale Silicon and non-Silicon technologies, low-power electronics for portable computing and wireless communications, VLSI testing and verification and reconfigurable computing. Dr. Roy has published more than 400 papers in refereed journals and conferences, holds 8 patents, and is co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill). Dr. Roy received the National Science Foundation Career Award in 1995, IBM faculty partnership award, ATT/Lucent Foundation award, 2005 SRC Technical Excellence Award and SRC Inventors Award. Dr. Roy is a fellow of IEEE.

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