Profit Aware Circuit Design Under Process Variations Considering Speed Binning

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***Abstract*—In this paper, a profit-aware design metric is proposed to consider the overall merit of a design in terms of power and performance. A statistical design methodology is then developed to improve the economic merit of a design considering frequency binning and product price profile. A low-complexity sensitivity-based gate sizing algorithm is developed to improve economic gain of a design over its initial yield-optimized design. Finally, we present an integrated design methodology for simultaneous sizing and bin boundary determination to enhance profit under an area constraint. Experiments on a set of ISCAS'85 benchmarks show in average 19% improvement in profit for simultaneous sizing and bin boundary determination, considering both leakage power dissipation and delay bounds compared to a design initially optimized for 90% yield at iso-area in 70-nm bulk CMOS technology.**

***Index Terms*—Design for profit, frequency-binning, gate-level sizing, leakage power, statistical delay variation.**

I. Introduction

EFFICIENT engineering design of a system is a complex process of selecting the most desirable design from a set of all feasible choices. From the integrated circuits (ICs) manufacturer's point of view, best measure of design merit is its profit, which is equivalent to excess of revenue over design cost, realized over a specified design cycle time [1]. In general, during design phase, profit is approximated as the expected economic gain resulting from the design and implementation of the product. However, presence of numerous design choices from different discrete design options (i.e., types of gates, logic style, device sizing, poly, and metal orientations) and continuous design parameters (i.e., area, delay, power) makes the economically justified design optimization a difficult problem. In semiconductor industry, design cycle time and market demands are among a few other sensitive parameters that significantly affects the economic gain [1].

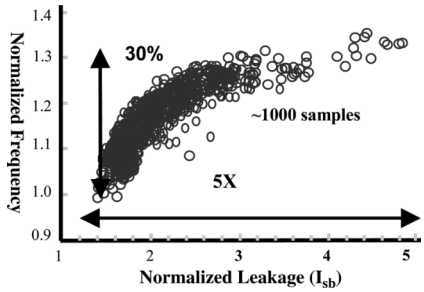

Fig. 1. Leakage and frequency variations of a high performance design in 130-nm technology (source: Intel).

Increasing variations (both inter-die and intra-die) in device parameters (channel length, gate width, oxide thickness, device threshold voltage, etc.) produce large spread in the speed and power consumption of integrated circuits [2], [3]. Consequently, parametric yield of a circuit (probability to meet the desired performance or power specification) is expected to suffer considerably. Due to exponential dependence of leakage power with the device threshold voltage $(V_{\rm th})$, parameter variations result in larger variability in leakage power. Fig. 1 shows the distribution of operating frequency and leakage current over a large number of high-end microprocessor chips [3]. It depicts that a mature silicon technology like 130 nm suffers from about 30% variation in maximum allowable frequency of operation and about $5\times$ variation in leakage power.

Economic merit of a design is conventionally equated with yield [2]. However, large spread in the operating frequency due to increasing uncertainties has led to the concept of speed binning to improve the design profit [4]. Presently, speed binning is widely used during manufacturing test to qualitatively sort the working (i.e., free from manufacturing defects) ICs based on their highest permissible frequency of operation. During the speed binning process, functional or structural tests are run at multiple frequencies and parts are binned according to the highest speed test they pass [4]. Since high-frequency ICs correspond to higher price points compared to their low-frequency counter parts, maintaining yield at a target circuit delay (i.e., frequency) under statistical delay distribution does not ensure maximum economic gain of the design.

Efficient design of high-performance circuits with high parametric yield under parameter variations has emerged as a major challenge in nano-scaled technologies [3], [11]. Recently, statistical timing analysis and leakage power estimation has been extensively explored in [5]–[8]. Several parametric yield

Manuscript received July 14, 2005; revised May 9, 2006 and June 14, 2007. This work was supported in part by Marco Gigascale System Research Center (GSRC), by Semiconductor Research Corporation (SRC), and by the National Science Foundation (NSF). A preliminary version of this paper titled "Speed Binning Aware Design Methodology to Improve Profit under Parameter Variation," was published in the Asia and South Pacific Design Automation Conference (ASP-DAC), 2006, pp. 712–717.

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Digital Object Identifier 10.1109/TVLSI.2008.2000364

estimation frameworks that consider the variability in circuit delay and leakage power are described in [5], [9], and [10]. At the same time, multiple efforts have been made to develop statistical design methodology to enhance and optimize parametric yield (e.g., with respect to delay and/or leakage power) [10], [12]. These works mostly focus on optimizing timing and/or leakage power yield. However, economic aspects of the design due to different power-performance specifications of the working products are not considered. Hence, there is a need to develop design methodology that can improve the design profit (instead of timing yield) under parameter variations.

In [1], Riley and Vincentelli presented an analytical modeling framework that targets to maximize the expected value of economic gain for statistical design of integrated circuits. However, [1] mainly focuses on modeling the manufacturing and design uncertainties for effective economic gain. A major contribution of our work is the optimization of design profit, considering frequency bins and product price profile. In particular, our work makes the following contributions:

- frequency bin price-weighted design metric that considers price of ICs running at different frequencies and satisfies power dissipation requirement;
- statistical design methodology to improve the profitability of a design using a sensitivity-based low-complexity gate sizing algorithm under both delay and power dissipation bounds;
- we have developed an integrated design flow for simultaneous gate sizing and optimal bin boundary determination to optimize design profit for a given price profile under an area constraint. The design methodology is based on tailoring the delay distribution in a way that places the right number of ICs in the right bin to maximize the profit.

Application of the proposed methodology to a set of ISCAS'85 benchmark circuits shows, in average 19% profit improvement over a 90% yield optimized design, without any area overhead, for three frequency bins in 70-nm BPTM [14].

The remainder of this paper is organized as follows. Section II gives a brief background on yield modeling and presents motivation for this work. A profit-aware design metric is described in Section III. Section IV presents a statistical design methodology using sensitivity-based gate sizing for profit improvement. In Section V, we propose an algorithm to simultaneously perform gate sizing and bin boundary placement for enhancing profit. We conclude this paper in Section VI.

II. Background and Motivation

Usually expected economic gain of a design is not the explicit criterion for the circuit optimization. The principal reason behind this is the absence of suitable economy aware design optimization model. Inclusion of explicit economic criterion in the design framework leads to the development of an attractive statistical design methodology. We, first introduce such an model to develop a profit-aware design framework.

A. Timing Yield Model

Under parameter variations, each gate has a delay distribution, which can be approximated as a Gaussian random variable instead of a single value [7], [8]. The delay of a timing path is the statistical sum of propagation delays through the combinational logic gates and interconnects in the path. Since the sum of two or more Gaussian variable is also a Gaussian, path delays are also Gaussian variables. Finally, circuit delay is the maximum of all path delays in the circuit, and can also be approximated as Gaussian distribution as explained in [7]. The overall circuit delay $T_{\rm ckt}$, thus follows a Gaussian distribution and can be modeled as a random variable with mean μ and standard deviation (STD) σ [i.e., $T_{\rm ckt} \sim N(\mu_i, \sigma_i)$]. Conventionally, timing yield (Y_T) of a design is defined as its probability to meet the target delay (T_D)

$$Y_T = Pr\{0 < T_{\rm ckt} \leq T_D\} = \int_0^{T_D} f_T(t)dt \tag{1}$$

where $f_T(t)$ is the probability density function (pdf) of the circuit delay.

B. Parametric Yield Model Considering Leakage Variation

In nano-scaled designs, leakage power of a circuit exhibits a strong correlation with circuit delay, resulting in parametric yield loss of the high speed lots of the product [5]. The yield loss is contributed by the faster devices with lower V_t (and/or lower channel length). These devices suffer from an exponential increase in subthreshold leakage. It implies that most of the fast chips will be too leaky and have to be discarded, even though they meet timing [5]. Mathematically, effective parametric yield $(Y_{\rm eff})$ considering leakage constraint can be expressed as

$$Y_{\rm eff} = Pr\{T_{\rm ckt} \leq T_D, P_{\rm leakage} \leq P_{\rm lim}\} \tag{2}$$

where $P_{\rm lim}$ is the leakage power dissipation constraint of the circuit. In Fig. 1, we observe that most of these leaky chips lie in the highest frequency spectrum for 130-nm technology node. We also find similar relationship between frequency and leakage variation in smaller technology nodes in [16]. This demonstrates strong correlation among the maximum operating frequency and leakage power dissipation of a circuit. In [5], Rao *et al.* show that with accurate full chip leakage power estimation, maximum leakage yield loss occurs in the highest frequency bin, while negligible (all together less than 3%) yield loss occurs in other frequency bins. In this paper, we use a minimum delay ($T_{\rm leakage}$) value as leakage power dissipation limit for parametric yield loss. This allows us to approximate yield loss due to excessive leakage as

$$Pr\{P_{\rm leakage} \leq P_{\rm lim}\} \approx Pr\{T_{\rm leakage} \leq T_{\rm ckt}\}. \tag{3}$$

Using $T_{\rm leakage}$ bound together with T_D in (1), effective yield of a design can be expressed as

$$Y_{\rm eff} \approx Pr\{T_{\rm leakage} \leq T_{\rm ckt} \leq T_D\} = \int_{T_{\rm leakage}}^{T_D} f_T(t)dt. \tag{4}$$

Results from recent works [9], [10] also corroborate this simplification. The authors of [9] and [10] have considered correlated variations of performance and leakage power to accurately estimate parametric yield under simultaneous leakage constraint and delay bound. Their results show that leakage power contributes to maximum yield loss in the highest frequency bin. Random components of the leakage power contribute to overall

2% and 4% yield loss, respectively, over the timing yield across other lower frequency bins. This implies that using a delay based leakage bound instead of accurate leakage power estimation, we compromise less than 4% accuracy in computation of Y_{eff}. For simplicity of analysis, we have used minimum delay (T_{leakage}) as a leakage power dissipation constraint. However, the proposed formulation is not limited by this assumption of T_{leakage} as a leakage power dissipation bound. It can be extended to consider different delay and leakage bounds in each frequency bin.

It is important to note that, besides leakage power, dynamic power consumed by logic circuit, clock, and memory part of the system also contributes towards the total power of the chip. Under a design area constraint on the circuit, clock power dissipation also remains unchanged. Assuming suitable techniques can be applied to improve memory power and parametric yield [22], this work focuses to improve profit based on logic power and performance of the system.

C. Design Considerations Under Process Variation

Fig. 2 shows two possible circuit delay distributions with three frequency bins for a test circuit c74181. Here, vertical axis represents the number of chips that lie in a small delay range (say 5% of the total delay window), out of total 10 000 random samples of the circuits, considering a Gaussian delay distribution. ICs with delay higher than T_D or lower than T_{leakage} are discarded. In Fig. 2, dashed line corresponds to the delay distribution for a parametric yield optimized design (at target delay T_D). The other distribution (solid line) is obtained by selective gate resizing of $\text{Yield}_{\text{optimized}}$ design in such a way to improve the economic gain of the design (also referred to as *design profit*) with respect to three discrete bin prices C_i. This plot represents the case where $\text{Yield}_{\text{optimized}}$ circuit have higher effective yield [according to (4)] with respect to T_D and T_{leakage}. However, design profit improves for $\text{Profit}_{\text{optimized}}$ design. In this case, yield loss suffered by $\text{Profit}_{\text{optimized}}$ design in lower frequency bins, is easily amortized by significant economic gain from the increased bin yield in the highest frequency. Based on the previous discussions, we observe the following.

- Design profit with respect to a price profile can be improved even at the cost of degrading effective parametric yield by suitably changing circuit delay distribution. It is important to distribute the parametric yield appropriately across the different frequency bins to optimize economic gain of the design. Most importantly, process variation if used effectively during the design phase, can be economically rewarding.

III. Profit-Aware Design Metric Under Process Variation

In semiconductor industry, profit (realized over a specified time interval) is the most appropriate representation of economic gain. Profit (Π) is defined as excess of revenue $(\Re)$ over its manufacturing cost [1]. This can be mathematically represented after [1] as

$$\Pi = \Re - \text{Cost} = R(e,p) - g(e,u) \tag{5}$$

where e is the set of electrical performance specifications of the design, u represents the set of design parameters (like device dimensions), and $g(e,u)$ represent the cost function. Finally, p denotes the prices at which the designed product is sold to the market and $R(e,p)$ denotes the design revenue. Fig. 3(a) shows a normalized price versus frequency plot of two recent high-end processors as obtained from [19]. We observe, for both the processors, price of the highest frequency part is about three times higher than that of the lowest frequency part. Under an area constraint the design cost, dominated by fabrication cost, remains practically constant [1]. Hence, for iso-area design, we can consider design revenue, as a measure of design profit (Π_D). Thus, considering N frequency bins, design profit can be expressed in terms of price-weighted cumulative sum of bin-yields as

$$\Pi_D = C_1 Y_{\text{bin1}} + \cdots + C_N Y_{\text{binN}} = \sum_{i=1}^{N} C(T_i) Y_{\text{bin\_i}}$$
$$\Pi_D = w_1 Y_1 + \cdots + w_N Y_N = \sum_{i=1}^{N} w_i Y_i \tag{6}$$

where $T_N = T_D =$ target design delay, and weighing parameter $w_i = C(T_i)$ is price of a chip in the ith frequency bin. Fig. 3(b) shows circuit delay distribution versus exponential product price profile with three frequency bins (i.e., $N = 3$) for an ISCAS'85 benchmark circuit c499, realized in 70-nm BPTM [14]. The delay distribution is computed considering both systematic and random variations in threshold voltage. We have considered $3\sigma_{V\text{th}}$ as 15% of the nominal V_{th}. As all the ICs in a frequency bin are sold at the same price, any product price profile essentially becomes a stair-case function of delay (or frequency) as shown in Fig. 3(b). Price points for the bins are constructed from the minimum bin frequencies. To achieve the similar bin price ratio [$\approx$3 as in Fig. 3(a)], for all circuits, we choose price weights (w_i) in such a way that ratio of the prices at the highest and lowest permissible frequencies is constant. Mathematically this can be represented as

$$\frac{w_{\max}}{w_{\min}} = \text{Constant} = R_{price\_profile} \tag{7}$$

where $w_{\min} = C(f_{\min})$, $f_{\min} = (1/T_D)$, $w_{\max} = C(f_{\max})$, and $f_{\max} = (1/T_{\text{leakage}})$. Four delay specifications (T_{leakage}, T_1, T_2, T_D) are used to consider three frequency bins in Fig. 3(b). Yield of ith frequency bin (Y_i) is defined as the fraction of the chips that lies within its specified delay (frequency) range. For example, yield of bin 1 (Y_1), is the fraction of the

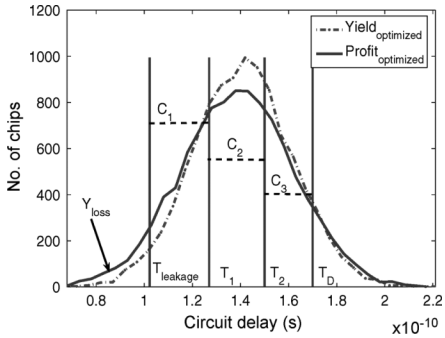

Fig. 2. Circuit delay distributions with $\text{Yield}_{\text{optimized}}$ design having higher effective yield than $\text{Profit}_{\text{optimized}}$ design.

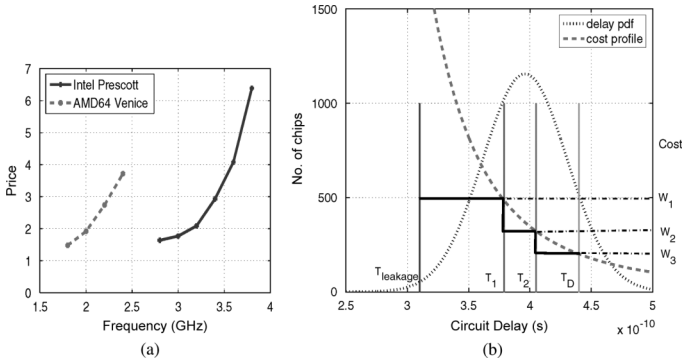

Fig. 3. (a) Price and frequency comparisons of two recent high-end processors. (b) Exponential price profile versus delay distribution for benchmark circuit c499.

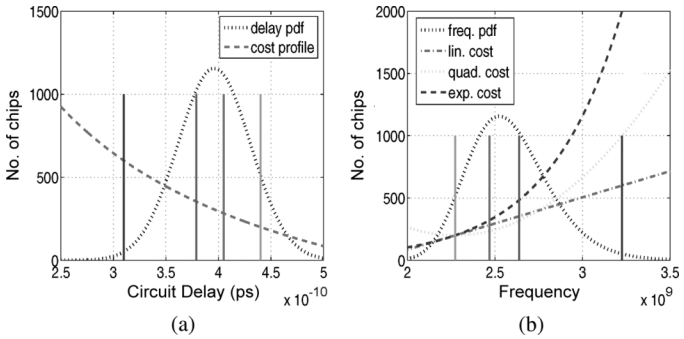

Fig. 4. (a) Linear price profile versus delay distribution. (b) Operating frequency versus different price profiles for c499.

chips having delay less than T_1 but higher than T_{leakage}. Assuming a Gaussian circuit delay distribution with mean (μ) and standard deviation (σ), different bin yields can be expressed as

$$Y_1 = \Phi\left(\frac{T_1-\mu}{\sigma}\right) - \Phi\left(\frac{T_{\text{leakage}}-\mu}{\sigma}\right)$$
$$Y_i = \Phi\left(\frac{T_i-\mu}{\sigma}\right) - \Phi\left(\frac{T_{i-1}-\mu}{\sigma}\right) \ \forall i = 2,\ldots,N \quad (8)$$

where $\Phi((T-\mu)/\sigma) = \int_0^T (1/\sigma\sqrt{2\pi})\exp^{-(x-\mu)^2/2\sigma^2}dx$.

In (6) and (7), price function C can represent any price profile depending on the design's market demand. In this paper, we have considered price profiles with linear, quadratic, exponential dependence on frequency. Any other types of price profiles, even discrete, piece-wise linear bin prices can also be incorporated in proposed profit-aware design optimization

$$w_{\text{lin}} = C_{\text{Linear}}(f) = m*f + K_1$$
$$w_{\text{quad}} = C_{\text{Quadratic}}(f) = a*f^2 + b*f + K_2$$
$$w_{\text{expo}} = C_{\text{Exponential}}(f) = K_3 e^{kf}. \quad (9)$$

Equation (9) shows three different price models, where m, a, b, k, K_1, K_2, and K_3 are design specific constants. A typical example of a linear profile for an ISCAS'85 benchmark circuit c499 is shown in Fig. 4(a). Fig. 4(b) plots three different price profiles versus operating frequency for this circuit.

A. Profit-Aware Gate Sizing Problem Formulation

The profit-aware design metric (6) can thus enable us to optimize net economic gain of high-performance circuits under variations instead of maximizing its parametric yield. Using (6), profit optimization problem with respect to a given price profile and N frequency bins can be formulated as shown in (10)

$$\text{Maximize } \Pi_D = \sum_{i=1}^{N} C\left(\frac{1}{T_i}\right) \int_{T_{i-1}}^{T_i} f_T(t)dt$$
$$\text{Subject to } A = \textstyle\sum_{i=1}^{n} x_i = \text{constant}$$
$$/* \text{ where} T_0 = T_{\text{leakage}};\ T_N = T_D; n = \text{circuit gate count}$$
$$A = \text{Total active area};\ x_i = \text{size of } i^{\text{th}} \text{ gate } */ \quad (10)$$

B. Statistical Delay Model

To compute the delay distribution of a circuit based on the information of both die-to-die and within-die parameter variations, we have employed the statistical static timing analysis (SSTA) algorithm proposed in [6] and [8]. The algorithm simultaneously considers the impact of random and the spatial correlation of the process parameters as well as the signal correlation due to reconvergent paths in the circuit. To compute the mean and standard deviation of gate delay, we have used a first order Taylor's expression as

$$D = D_0 + \sum_{i}^{n} s_i X_{V_t,i} + s_L X_L \quad (11)$$

where $s_i = (dD/dV_{t,i})$, and $s_L = (dD/dL)$. In (11), D_0 represents nominal gate delay without any variation, n is the number of transistors in the gate. $X_{Vt,i}$ and X_L are Gaussian random variables representing variation in transistor threshold voltage and channel length, respectively. Nominal delay (D_0) is modeled using analytical expression presented by Sakurai *et al.* [15]. The sensitivity values $(s_i,\ s_L)$ are obtained from a set of devices generated using MEDICI [20] device simulator. For simplicity, we ignore interconnect delays, but our algorithm can be extended to incorporate interconnect delays using conventional resistance–capacitance (*RC*) model as used in [13].

IV. Profit-Aware Design Optimization

To cope with the increasing yield loss due to process parameter variations, effects of manufacturing variations are already considered during the design phase [2], [5]. Conventionally, product price profile is used in the testing phase during frequency binning. In this paper, we demonstrate the use of product price information with respect to frequency bins in the design optimization phase can maximize design profit.

A. Yield Optimization for a Target Delay Using Gate Sizing

Gate sizing is conventionally used in circuit synthesis tools for area/power optimizations while meeting a desired timing constraint, or for minimizing the maximum delay under constraint on area/power [13]. We use a gate-level sizing algorithm as proposed in [13] using Lagrangian relaxation (LR)-based nonlinear optimization to minimize active design area under a

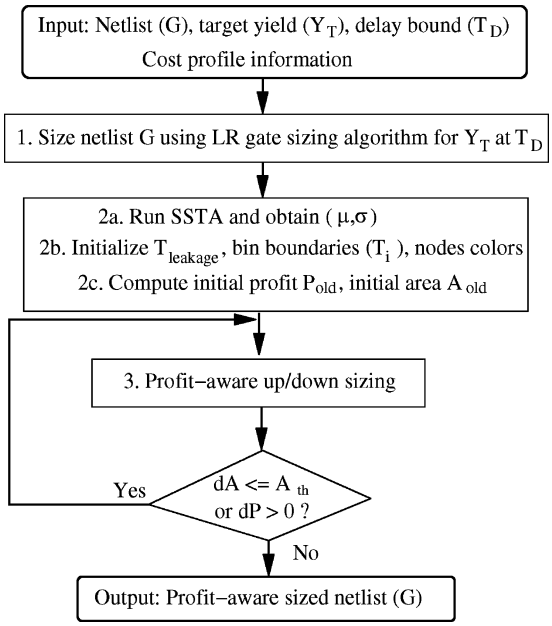

Fig. 5. Profit-aware statistical gate sizing algorithm.

constraint on maximum delay. Since total number of paths in a circuit varies exponentially with component count in a circuit (gate and wire segments), LR-based sizing approach employs the classical technique of partitioning path delay constraints into constraints (which is polynomial in the number of components) on delay across logic gates and wire segments. Then it solves the resultant problem by LR. Mathematically, gate sizing problem to achieve mean delay τ_0 with minimum area can be formulated in reference to (10) as

$$\begin{aligned} &\text{Minimize } \textstyle\sum_{i=1}^{n} x_i; \\ &\text{Subject to } \textstyle\sum_{i\in p} \text{mean}(D_j) \le \tau_0,\ \forall p \in P \text{ and} \\ &\qquad L_i \le x_i \le U_i \\ &\text{Timing yield}(Y_T) \ge Y_{\text{Target}} = Y_{\text{eff}} + Y_{\text{Loss}} \\ &\Rightarrow \textstyle\int_0^{T_D} f_T(t)dt \ge Y_{\text{Target}} \end{aligned} \tag{12}$$

where P denotes the set of all the circuit paths, D_j is the delay of the jth gate in a path $p \in P$, and L_i and U_i represent the lower and upper limit of the gate size, respectively. We initialize all gates with minimum size for our proposed gate sizing algorithm. It iteratively achieves a sizing solution that satisfies the timing constraints of (12). Let us consider the mth sizing iteration of this sizing scheme. Mean target delay obtained after SSTA is μ_m (σ_m is the STD). This mean delay target is then updated in small steps to meet final yield target [12]. For example, at the next iteration, μ_m^{new} is set to μ_{m+1}, such that a feasible sizing solution can be expressed as

$$\begin{aligned} \int_0^{T_D} f_T(t)dt &= \Phi\left(\frac{\tau_0 - \mu_{m+1}}{\sigma_{m+1}}\right) \ge Y_{\text{Target}} \\ \mu_{m+1} &\le \tau_0 - s\sigma_m \Phi^{-1}(Y_{\text{Target}}) \end{aligned} \tag{13}$$

where $\sigma_{m+1} = s\sigma_m$ and μ_{m+1} are feasible mean and STD of the circuit delay in the $(m+1)$th iteration. $s < 1$ is a factor that controls the speed of convergence.

B. Profit-Aware Gate Sizing

We propose a sensitivity-based profit-aware gate sizing methodology to improve the design profit from an initial yield-optimized design at iso-area. Fig. 5 shows principal steps of our profit-aware sizing methodology. Step 1 has been detailed in Section IV-A. Once the design is optimized for parametric yield with minimum area, we perform SSTA to determine the delay distribution parameters (Step 2a). Under iso-area design optimization dynamic power dissipation of the circuit also remains constant. Hence the chip power budget is determined by the leakage power dissipation only. We define leakage bound based on delay distribution parameters (μ, σ) of yield-optimized design as

$$T_{\text{leakage}} = f(\mu, \sigma) = \mu - (l * \sigma) \tag{14}$$

where l is a constant. With this definition of T_{leakage} even when delay distribution parameters vary with sizing, the leakage bound does not change. Hence, the problem formulation in (10) remains valid independent the of delay parameter values. We then initialized the bin boundaries so that Y_{eff} is equally distributed among the N bins as

$$\begin{aligned} Y_{\text{Target}} &= \int_0^{T_D} f_T(t)dt = \Phi\left(\frac{T_D - \mu}{\sigma}\right) \\ \Rightarrow T_D &= \Phi^{-1}(Y_{\text{Target}}, \mu, \sigma) \\ Y_{\text{bin}} &= \frac{Y_{\text{Target}} - Y_{\text{leakage}}}{N} \\ \Rightarrow T_i &= \Phi^{-1}\left((Y_{\text{leakage}} + iY_{\text{bin}}), \mu, \sigma\right) \\ &\qquad \forall i = 1, \ldots, N. \end{aligned} \tag{15}$$

However, it should be noted that, initial bin boundaries can be anything and need not follow any particular distribution. Later, we present results with a more generic design framework demonstrating the effect of changing bin boundaries on the extent of profit improvement.

We then compute initial design profit P_{old} and initial design area A_{old} (computed as active area) for the particular delay parameters (μ, σ). In Step 3, we perform profit-aware gate-sizing under an area budget. Table I shows pseudo-code for our sensitivity-based up/down sizing routine. The routine is called once in each iteration of the sizing flow (see Fig. 5). The basic task is to choose a set of sensitive gates in the design for either up or down sizing. We apply sizing step (satisfying the upper and lower size limits, U_i and L_i, respectively) to these gates and perform SSTA to recompute the delay distribution. A gate with higher sensitivity is sized before the gates with lower sensitivities.

The run-time complexity of this overall profit-aware sizing algorithm depends on the number of SSTA calls in sensitivity analysis during an up/down sizing iteration. In this routine, we have employed the following two optimization techniques to improve the runtime (complexity) of the proposed gate sizing method by reducing the number of SSTA calls.

1) We perform profit sensitivity (S_P) computation of all gates in $\{S_C\}$ by changing one gate size at a time, with a small step (dx) and computing the corresponding change in profit (i.e., $S_P = dP/dx$). The sensitivity analysis is performed

TABLE I
PSEUDO-CODE FOR UP/DOWN SIZING

up-downSizing()
Input: Netlist (G)
Output: Sized netlist (G) after one sizing iteration
Direction: down = 0; up = 1
1. Compute profit sensitivity of all gates;
2. Select gates $\{S_C\}$ from critical set of paths;
3. Remove the gates with unacceptable profit sensitivity form $\{S_C\}$;
4. Sort gates of set $\{S_C\}$ in the descending order of profit sensitivity;
5. while (not all gates are colored)
6. Choose the most sensitive uncolored gate;
7. Size the gate by dx in proper direction;
8. Color its fan-in and fan-out logic cone;
9. end //while
10. Reset color of all gates;
11. Perform SSTA (G) to obtain $\mu^{'}, \sigma^{'}$
12. $P_{new} = P(T_0, T_1, \cdots, T_N, \mu^{'}, \sigma^{'})$;
13. $dP = P_{new} - P_{old}$;
14. $P_{old} = P_{new}$;
15. $dA = Area(G) - A_{old}$;

for both sizing directions (i.e., up and down). If a logic gate has unacceptable profit sensitivities (i.e., profit drops with upsizing or degrades too much with down sizing) in an iteration, we remove it from the selection set $\{S_C\}$ in the subsequent calls of up/down sizing (line 3 of Table I).

2) Multiple up/down sizing steps can be performed after each sensitivity analysis by selecting successive gates not lying in the fan-in and fan-out logic cone of the previously sized gates. In each iteration, we color the fan-in and fan-out cone of a sized logic gate in the graph (G) (line 8 of Table I). The colored nodes are not considered for sizing in an iteration. When no suitable uncolored gate exists in $\{S_C\}$, the iteration terminates. We then mark all gates uncolored and perform a SSTA to update the increment of profit (dP) and area (dA) values of the given circuit (lines 10–15 of Table I).

These two techniques jointly reduce the average number of gates that undergoes profit sensitivity analysis in an iteration with negligible degradation (less than 1%) in the overall profit improvement compared to a case where sensitivity analysis is performed for all gates. It is important to note that, we perform downsizing of the least profit sensitive gates to partially recover from the area overhead incurred during upsizing phase such that the area constraint $A_{\text{th}} \approx 0.3\%$ of A_{old} is satisfied. It is worth noting that, aggressive upsizing of the overall design can also maximize yield at high-frequency bins to optimize overall design profit at the target delay (T_D). However, it comes with large area (and hence power) penalty which affects the assumption of simplified timing based leakage bound (T_{leakage}). With excess dynamic power dissipation, leakage power limit reduces under a constant design power budget (see Fig. 6). This causes large leakage yield loss in high-frequency bins due to higher design area and reduced leakage power limit. Hence, design profitability drops significantly if we aggressively shift the circuit delay distribution towards higher frequency region (see Fig. 6, the dashed curve). In Fig. 6, we plot the delay distributions for

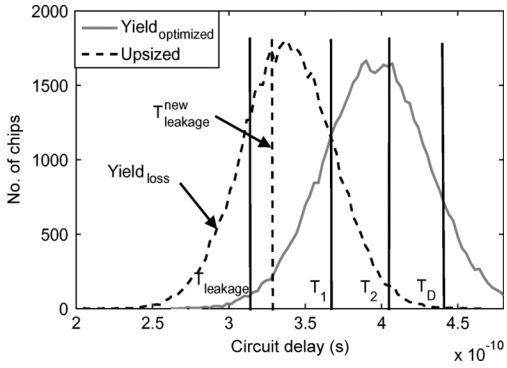

Fig. 6. Circuit delay distributions of c499 for different design objectives.

TABLE II
PROFIT-AWARE DESIGN RESULTS COMPARED TO 90% YIELD-OPTIMIZED DESIGN $(N = 3)$

Circuit	Target delay T_D (ps)	Profit improvement (%) $R_{Lin}=3$	$R_{Quad}=5$	$R_{Expo}=10$	% Y_{loss} (Expo.)	t_{iter} (second)	N_{iter}	t_{total} (second)
c432	520	9.53	9.20	12.80	1.36	1.15	3	3.44
c499	440	7.75	8.58	9.66	0.88	15.38	4	61.51
c880	400	16.28	15.16	20.89	1.06	7.99	8	63.91
c1908	520	7.02	6.50	9.07	0.14	9.93	6	59.59
c2670	425	8.11	7.15	10.32	1.14	52.05	5	260.24
c3540	640	18.78	18.04	26.18	1.60	57.66	5	288.29
c6288	1725	12.98	12.04	17.89	1.87	42.47	21	891.79
c74181	200	7.27	6.49	9.28	1.04	0.25	2	0.50
c74L85	150	2.77	2.57	3.53	0.73	0.05	2	0.09
c74283	170	13.83	13.29	19.06	2.12	0.09	2	0.17
Average		10.43	9.92	14.15	1.19	18.70	6	162.95

two different sizing solutions of a benchmark circuit c499. Considering an exponential cost profile, we observe that upsized design incurs about 20% area penalty to achieve comparable design-profit with respect to a profit-aware deterministic sizing solution.

C. Complexity of Profit-Aware Sizing Algorithm

Our complete design procedure consists of two phases: 1) LR-based sizing and 2) sensitivity-based profit-aware sizing. The computation complexity of LR-sizing is $O(n^a)$, where n is the number of gates in the circuits and $a \approx 1.7$ [13]. The complexity of SSTA algorithm used in our work is expressed as $\sum_i^m 0(n_i^2)$, where m is the logic depth of given circuit and n_i is the number of gates in the ith logic level [6]. Since SSTA is a computationally intensive algorithm, the overall execution time of profit-aware sizing algorithm is mostly determined by the number of SSTA function calls. We reduce the number of SSTA calls by discarding unsuitable gates for sizing from the candidate pool (see Section IV-B). The profit-aware sizing takes 0.09 s for the smallest benchmark (c74L85, 33 gates) and about 15 min for the largest benchmark (c6288, 2503 gates), other results can be found in Table II. All the simulations have been run on a Linux server with 3.06 GHz Pentium Xeon processor and 2 GB RAM.

The speed binning technique is usually employed on aggressively pipelined high performance systems like microprocessors. These high performance systems has about 5–10 levels of logic in each stage, the gate count in each logic stage, will be comparable to that of c6288 benchmark circuit. Thus, optimizing individual logic stage at a time can efficiently partition the sizing problem for a large system. Note that we can apply incremental timing analysis (realized by incremental timing refinement considering only the gates with modified size) [21] for

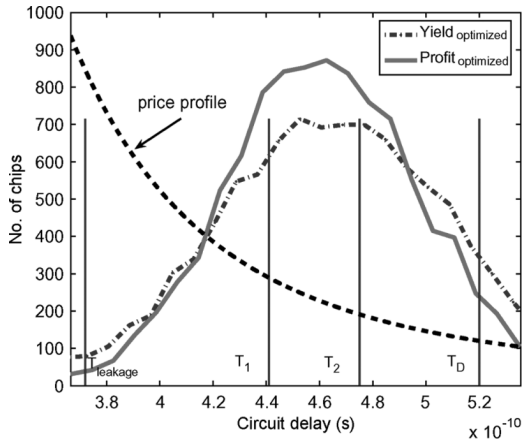

Fig. 7. Circuit delay distributions change due to profit-aware sizing for c1908 with $T_{\text{leakage}} = \mu - 2.5\sigma$ considering an exponential price profile.

a large number of SSTA runs to improve the runtime further. The incremental timing analysis [21] can be performed for all calls to SSTA during sensitivity analysis of gates (see Table I).

D. Experimental Results

We have applied the proposed profit-aware statistical design on several ISCAS'85 benchmarks for different number of frequency bins. We have considered design profit improvement under three different price profiles with price ratios as defined in (7): 1) linear $(R_{\text{lin}} = 3)$; 2) quadratic $(R_{\text{quad}} = 5)$; and 3) exponential $(R_{\text{expo}} = 10)$. The design profit (Π_D) is then computed using (6). The bin boundaries are quantized to the nearest picosecond of delay. We initialize fixed bin boundaries in such a way that all frequency bins have equal yields. However, this equal yield frequency bin condition is later relaxed to achieve more profit improvement (see Section V). The profit improvements for three frequency bins are reported in Table II. Columns 3–5 present profit improvement for different price profiles as a percentage of profit for a design that just meets 90% yield requirement (henceforth, we refer it as $Y_{\text{optimized}}$ design) with $T_{\text{leakage}} = \mu - 2.5\sigma$.

Using the proposed method, we obtain up to 26% profit improvement (for c3540 benchmark). Overall, we observe about 10.4% profit improvement for the linear, about 9.9% for the quadratic, and about 14.2% improvement for the exponential price profile at iso-area (see Table II) for ISCAS'85 benchmarks. Column 6 reports % yield loss of profit optimized design due to leakage bound considering exponential price profile. Average runtimes (t_{iter}) for one profit-aware sizing (see Table II) iteration considering exponential price profile are reported in column 7 for all the circuits. Similar runtimes are observed for the other price profiles since they are dominated by the number of calls to the SSTA routine. The number of sizing iterations (N_{iter}) required by the proposed sizing scheme varies from 2 to 21 with an average of 6 (see column 8).

Fig. 7 plots the delay distributions for a benchmark circuit, c1908 before and after profit-aware sizing along with the exponential price profile used for the particular benchmark. With profit-aware gate sizing, design profit improves by about 9.07% (see Fig. 7).

Profit improvement varies widely across the benchmarks and it largely depends on the design specifications as well as on the circuit topology (see Table II). To observe the effect of initial yield target variation on profit improvement, we have obtained three sets of average profit improvement results for three different Y_{Target} values. It is observed that, the scope of profit optimization decreases with the increase in Y_{Target} [see Fig. 8(a)]. Fig. 8(b) shows profit improvement with different leakage bounds are quite similar. The scope of profit improvement for a given price profile increase with the relaxed leakage bounds. Fig. 9 shows profit improvements for various benchmarks as the number of frequency bins is varied under an exponential price profile. Note that we have not considered the smaller benchmarks (c74181, c74L85, c74283) in this plot since they have small delay spread (see Table II). The trend of increasing profit improvement with the number of bins can be attributed to the fact that with fine-grained frequency binning, the high frequency bin prices (and the average bin price) increase considerably under a given price profile.

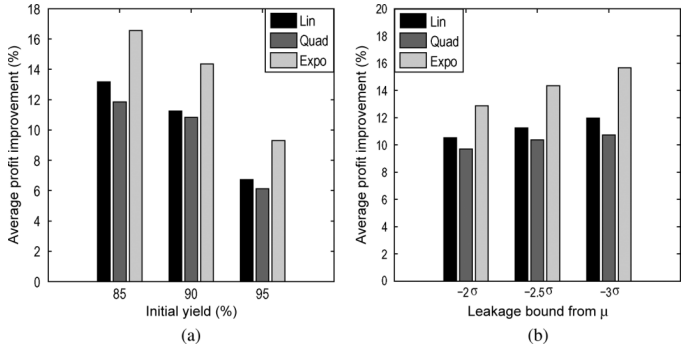

Fig. 8. Average profit improvement with three bins different (a) initial Y_{target} and (b) T_{leakage} for a set of ISCAS'85 benchmarks.

TABLE III
PSEUDO-CODE FOR OPTIMAL BIN BOUNDARY DETERMINATION

```
findOptBinBoundary()
 Input: Number of bins (N), delay params: μ, σ
 Output: Optimal bin boundaries (T_0, ..., T_N = T_D)
1.   Find equal yield bin boundaries (T_0, ..., T_N) for N bins
2.   P_old = P(T_0, T_1, ..., T_N, μ, σ)
3.   while (no change in T_i )
4.       for each T_i (0 < i < N)
5.           P_new+ = P(..., T_i + dT, ..., T_N, μ, σ);
6.           dP+ = P_new − P_old;
7.           P_new− = P(..., T_i − dT, ..., T_N, μ, σ);
8.           dP+ = P_new − P_old;
9.           if (dP+ > 0)
10.              T_i = T_i + dT; P_old = P_new+;
11.          else if (dP− > 0)
12.              T_i = T_i − dT; P_old = P_new−;
13.          end //if
14.      end //for
15.  end //while
```

V. Simultaneous Sizing and Optimal Bin Boundary Determination

In the profit optimization problem presented in (10), we assumed that the frequency bin boundaries are fixed and will be given to the designer. However, in case the bin boundaries are not available or designers are allowed to change them, they can

TABLE IV
SIMULTANEOUS PROFIT-AWARE SIZING AND OPTIMAL BIN DETERMINATION RESULTS FOR THREE BINS

Circuit	Target delay (ps)	Profit improvement (%)								
		Linear ($R_{lin}=3$)			Quadratic ($R_{quad}=5$)			Exponential ($R_{expo}=10$)		
		Fixedbin	Optbin	Addl. imp	Fixedbin	Optbin	Addl. imp	Fixedbin	Optbin	Addl. imp
c432	520	9.53	9.98	0.33	9.20	15.58	6.38	12.80	17.98	5.18
c499	440	7.75	8.01	0.26	8.58	14.58	6.00	9.66	13.13	3.47
c880	400	16.28	17.01	0.73	15.16	22.63	7.47	20.89	27.17	6.28
c1908	520	7.02	7.13	0.11	6.50	8.32	1.82	9.07	9.52	0.45
c2670	425	8.11	8.59	0.48	7.15	13.17	6.02	10.32	14.68	4.36
c3540	640	18.78	20.97	2.19	18.04	30.00	11.96	26.18	36.31	10.13
c6288	1725	12.98	14.02	1.04	12.04	20.69	8.65	17.89	26.07	8.18
c74181	200	7.27	7.66	0.39	6.49	11.93	5.44	9.28	13.30	4.02
c74L85	150	2.77	2.93	0.16	2.57	6.59	4.02	3.53	6.06	2.53
c74283	170	13.83	14.85	1.02	13.29	22.48	9.19	19.06	27.60	8.54
Average		10.43	11.11	0.67	9.92	16.70	6.70	14.15	18.78	5.31

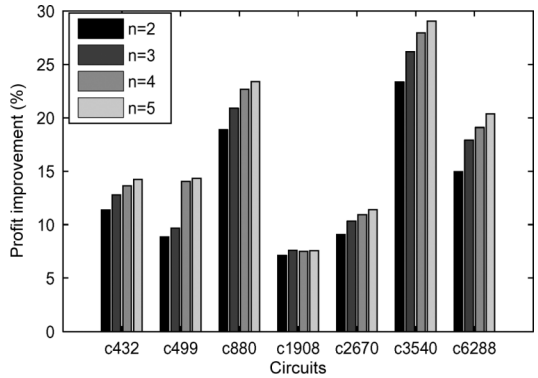

Fig. 9. Profit improvement of different number of bins for fixed bin boundaries with $T_{\text{leakage}} = \mu - 2.5\sigma$.

be chosen appropriately such that the profit metric is optimized for a given price profile.

A. Optimal Bin Boundary Determination

The problem of choosing the most profitable bin boundaries for a delay distribution can be formulated as follows: *given a circuit delay distribution, power, and performance specifications, determine the optimal frequency bin boundaries and transistor sizing to maximize the design profit under a particular price profile*. We assume that the number of frequency bins is fixed (say N). For N bins, given a delay distribution D and price profile C, the problem of finding optimal $N-1$ bin boundaries can be expressed as

$$\begin{aligned} &\text{Maximize } \Pi_D = \textstyle\sum_{i=1}^{N} C(T_i)(Y_i) \\ &\text{Subject to : } T_{\text{leakage}}(T_0) \leq \cdots \leq T_i \leq \cdots \leq T_N(T_D). \end{aligned} \tag{16}$$

In order to solve the problem of optimal bin boundary determination (16), we start with equal yield bin boundaries as defined in (15). We employ a greedy approach, where we pick one bin boundary at a time, to be altered for optimizing the design profit keeping other boundaries fixed. First, we search the optimal boundary for the highest allowable frequency bin as it can have the most impact in improving the profit. We repeatedly perform such optimization for other bins in descending order of frequencies. At the end, we obtain modified boundaries for all the bins that locally optimize the profit. The pseudo-code for optimal bin boundary determination is given in Table III.

We determine optimal frequency bin boundaries for the same set of ISCAS'85 benchmarks and computed corresponding profit improvements over fixed equal bin boundaries for different number of frequency bins. It is important to note that this technique does not have any design overhead. It only requires an extra design step to be incorporated after the final up/down sizing routine (see Table I).

B. Simultaneous Sizing and Bin Boundary Determination

We have combined optimal bin boundary determination and profit-aware sizing routine to develop an integrated design methodology that simultaneously perform gate sizing along with optimal bin boundary determination. Basic steps of the design flow are similar to that shown in Table I. The only difference is that, now we use optimal bin boundaries for profit sensitivity computation during the up/down sizing routine (Step 2 in Table I).

This method when employed to different ISCAS'85 benchmarks shows up to 36% profit improvement with three frequency bins (see Table IV), considering a leakage bound of $\mu - 2.5\sigma$ for an 90% yield-optimized design at equal area. For all price profiles, profit improvements for simultaneous sizing and optimal bin boundaries are shown under *Optbin* column, and additional profit improvements with simultaneous sizing and bin placement over fixed bin boundaries are under *Addl. imp* columns in Table IV.

As explained earlier, profit for linear price profile does not improve much compared to fixed bin approach with this integrated solution. However, the current approach shows significant profit improvement compared to fixed bin boundary results for both quadratic (from 10% to 16.7% on average) and exponential price profiles (from 14.1% to 18.8% on average) for the ISCAS'85 benchmarks (see Table IV). Fig. 10(a) shows the effectiveness of three proposed profit-aware sizing methodologies (i.e., fixed bin based sizing, fixed bin sizing + optimal bin boundary determination and simultaneous sizing and optimal bin boundary determination) for different price functions with $T_{\text{leakage}} = \mu - 2.5\sigma$. Fig. 10(b) shows consistent profit improvement with simultaneous sizing and optimal bin boundary determination for exponential price profile with increasing number of bins. Since optimal bin boundary determination routine has negligible runtime compared to SSTA routine runtime. The runtime

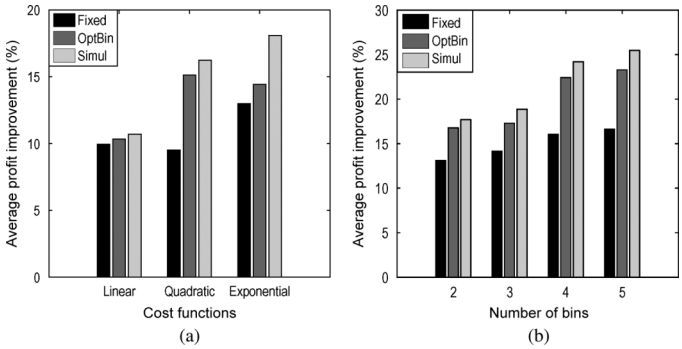

Fig. 10. Average profit improvement for (a) three price functions by sizing with different methods ($N = 3$) and (b) simultaneous sizing and optimal bin placement with different number of bins (exponential price profile).

of this integrated algorithm is similar to the runtime of sizing for profit optimization with fixed bin boundaries (see Table II).

It is worth noting that the proposed sizing methods (simultaneous profit-aware sizing and bin boundary determination) are useful to maximize profit for any price profile. Although we have considered Gaussian (normal) delay distribution models, the proposed design methods can be extended to non-normal delay distribution model [18].

VI. Conclusion

We have proposed a profit-aware design metric that considers power dissipation and performance variations across all the functional chips. Using the profit-aware design metric, we have developed a statistical design methodology to optimize design profit for a given price profile under an area constraint. We have implemented the proposed design methodology using a low-complexity sensitivity-based gate sizing algorithm. We have demonstrated that optimal bin-boundary determination can be used to increase the design profit. Our analysis shows that proposed profit-aware design flow that incorporates information on price profile and frequency binning during the design phase can be very effective in maximizing design profit under parameter variations.

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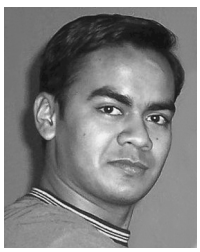

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