Low-Power and Testable Circuit Synthesis Using Shannon Decomposition

SWAROOP GHOSH, SWARUP BHUNIA, and KAUSHIK ROY
Purdue University

Structural transformation of a design to enhance its testability while satisfying design constraints on power and performance can result in improved test cost and test confidence. In this article, we analyze the testability in a new style of logic design based on *Shannon's decomposition* and *supply gating*. We observe that the tree structure of a logic circuit due to Shannon's decomposition makes it intrinsically more testable than a conventionally synthesized circuit, while at the same time providing an improvement in active power. We have analyzed four different aspects of the testability of a circuit: a) IDDQ test sensitivity, b) test power during scan-based testing, c) test length (for both ATPG-generated deterministic and random patterns), and d) noise immunity. Simulation results on a set of MCNC benchmarks show promising results on all these aspects (an average improvement of 94% in IDDQ sensitivity, 50% in test power, 19% (21%) in test length for deterministic (random) patterns, and 50% in coupling noise immunity). We have also demonstrated that the new logic structure can improve parametric yield (6% on average) of a circuit under process variations when considering a bound on circuit leakage.

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1. INTRODUCTION

Aggressive scaling in transistor geometries to meet the increasing demand on performance and device integration density has posed several challenges to the

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Authors' address: S. Ghosh (contact author), S. Bhunia, K. Roy, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907; email: ghosh3@purdue.edu.

test professionals. New failure mechanisms have emerged in logic as well as memory units due to parameter variations in nanoscaled circuits. Therefore, to enable efficient testing of nanoscaled devices and to improve yield, new approaches in test methodologies and design-for-testability (DFT) are required [Kundu 2000]. Quiescent current (IDDQ) testing has long been used to detect bridging faults in a circuit. However, relentless device scaling has largely deteriorated the subthreshold and gate tunneling leakage to such a level that it has become difficult to distinguish between the fault-free and faulty currents. Test power has also emerged as an important design concern to increase battery lifetime in handheld electronic devices. Another issue related to testing of nanometer circuits is test coverage due to increased defect density and new failure mechanisms. Along with the mentioned test issues, crosstalk adds another dimension to the problem. We believe that an integrated DFT solution is required that can reduce the test time and test power while maintaining the test coverage and alleviate the effects of signal integrity and process parameter variations. In this article, we have demonstrated that a new circuit synthesis style, based on Shannon expansion, can improve the testability of a circuit significantly while achieving low active power dissipation [Bhunia et al. 2005].

The remainder of the article is organized as follows. In Section 2, we provide an overview of the Shannon Expansion-Based Supply-gating synthesis (SBS) approach. In Sections 3–6, we present the application of SBS in improving IDDQ sensitivity, test power, test length, and coupling noise immunity. The limitations are discussed in Section 7 and conclusions are drawn in Section 8.

2. BACKGROUND ON SHANNON-BASED SYNTHESIS

2.1 Shannon Expansion and Dynamic Supply Gating Scheme

Shannon expansion has been used in logic synthesis for logic simplification and optimization [Lavagno et al. 1995]. It partitions any Boolean expression into disjoint subexpressions as follows:

$$\begin{aligned} f(x_1, \ldots, x_i, \ldots, x_n) &= x_i . f(x_1, \ldots, x_i = 1, \ldots, x_n) + \bar{x}_i . f(x_1, \ldots, x_i = 0, , x_n) \\ &= x_i . CF_1 + \bar{x_i} . CF_2, \end{aligned}$$

where x_i is called the *control variable*, and CF_1 and CF_2 are called *cofactors*. This expression implies that only one cofactor performs active computation, while the other cofactors perform redundant computations and leaks at any given time instant. This provides an opportunity for gating the supply of the idle cofactors (using control variable x_i) to reduce power due to redundant computations and leakage current [Bhunia et al. 2005].

2.2 Selection of Control Variable for Cofactor Balancing

Control variable selection for partitioning should be done to balance the resulting cofactors. Balancing of cofactors ensures that the circuit exhibits a similar amount of static current for any test vector. If a (b) is the number of literals associated with x_i ($\bar{x}_i$), then a control variable can be chosen to maximize M_i,

where M_i is given by

$$\begin{aligned} M_i &= (a+b)/(|a-b|) \quad \forall a! = b \\ &= (a+b) \text{ for } a = b \end{aligned}$$

In this expression, balancing of cofactors is imposed by the term $|a-b|$. Based on the synthesis procedure presented, we generate the SBS circuit and study its IDDQ sensitivity, test power, test length, and noise immunity.

3. IMPROVEMENT IN IDDQ SENSITIVITY

To measure the effectiveness of our technique, we define IDDQ sensitivity as $S = (I_f - I_g)/I_g$, where I_f (I_g) is the faulty (fault-free) IDDQ current. Therefore, sensitivity can be improved by reducing the background leakage current. In the proposed SBS method, leakage can be reduced significantly because, for a given test stimuli, only one cofactor does useful computation, while the idle cofactors are supply gated.

To verify the effectiveness of the proposed approach, experiments are performed on a set of MCNC benchmark circuits using a test setup as mentioned in Ghosh et al. [2005]. To obtain the SBS circuit for all experimental results presented in this article, the guidelines followed are: (a) cofactors are balanced; (b) shared logic size is small compared to other gated cofactors. If this is not true, then one more level of expansion is performed; and (c) the overall area (delay) penalty of SBS circuit is kept within 5% (2%) limit. We observed an average improvement of 94.4% in IDDQ sensitivity using the SBS technique. We also combined our method with the reverse body biasing technqiue for fair comparison. The results suggest that, when SBS is combined with body biasing, an average improvement of 37% in IDDQ sensitivity is achieved. To observe the effect of variation on IDDQ distribution of ORG and SBS circuits, we performed 10,000 runs of monte-carlo simulations in Hspice for different process corners. The average yield improvement for the proposed technique was found to be 6.25%. The details of simulation and results are described in Ghosh et al. [2005] and not presented here for the sake of brevity.

4. IMPROVEMENT IN TEST POWER

To observe the test power of ORG and SBS circuits, we model them in Hspice with BPTM 70nm technology devices as mentioned in Ghosh et al. [2005]. The simulation indicates that as much as 74.1% of test power can be saved with the proposed SBS technique. The average improvement in test power over all the benchmarks considered is about 50.5%. The details of simulation and results are described in Ghosh et al. [2005].

5. IMPROVEMENT IN TEST COVERAGE/TEST LENGTH

In this section, we study the effectiveness of the proposed SBS technique in reducing test length both for ATPG-based as well as BIST-based testing methods. We followed a similar test setup as in Ghosh et al. [2005]. We observed that a maximum of 41% (44%) improvement in test length for deterministic

Table I. Improvement in Testability for Stuck-at Test

	Stuck-0			Stuck-1		
Ckt	T(ORG)	T(SBS)	%imp	T(ORG)	T(SBS)	%imp
cht	1.22	1.39	13.93	1.42	1.34	−5.63
cm150a	0.64	1.07	67.18	0.65	1.09	67.69
mux	0.72	1.01	40.27	0.7	0.95	35.71
sct	0.82	1.17	42.68	0.79	1.21	53.16
decod	0.95	1.05	10.52	1.06	1.2	13.20
alu2	0.61	0.82	34.42	0.67	0.84	25.37
count	0.85	1.22	43.52	0.92	1.32	43.47
pcle	1.01	1.15	13.86	0.96	1.17	21.87
x2	0.66	1.2	81.81	0.67	1.23	83.58
Avg.			38.69			37.60

(random) patterns. The average improvement for deterministic (random) pattern is 19.7% (21.1%). The reduction in test length is because of the following two reasons: (1) the area of SBS is reduced after multilevel expansion in some cases leading to a fewer number of faults and (2) the increased testability of the internal nodes. This is because the control variables have been isolated during expansion and added to the select lines of MUXes near the primary outputs. The details of simulation and results are described in Ghosh et al. [2005].

To study the impact of the proposed synthesis approach on the testability of internal nodes, we compared the average testability of SBS circuits with the ORG circuits. The testability of an ith node is defined as in Bushnell and Agarwal [2000]: $T_0(i) = (C_1(i) + O(i))$ and $T_1(i) = (C_0(i) + O(i))$ where, $T_0(i)$ ($T_1(i)$) is the stuck-at 0 (stuck-at 1) testability, $C_0(i)$ ($C_1(i)$) is the 0 (1) controllability, and $O(i)$ is the observability of the ith node [Brglez 1984]. We depict the average testability of SBS and ORG circuits in Table I. It can be observed that except for benchmark *cht*, all other circuits show significant improvement in testability leading to an average improvement of 38.6% (37.6%) in stuck-at 0 (stuck-at 1) testability. The improvement in results indicate that for the similar functionality, test generation for SBS circuits is easier than ORG circuits.

6. IMPROVEMENT IN NOISE IMMUNITY OF THE CIRCUIT

In this section, we study the noise immunity of the SBS circuit compared to the ORG circuit. We show that the proposed technique intrinsically improves the noise immunity of the circuit. A simple example of noise in an ORG circuit is shown in Figure 1(a). It can be observed that the output can be affected by several interwire coupling capacitors. On the other hand, from Figure 1(b), we observe that in SBS circuits the coupling capacitors are naturally partitioned into inter-cofactor and intra-cofactor capacitors. It is interesting to observe that due to the supply gating of cofactors, the inter-cofactor coupling capacitors from idle cofactors cannot create noise in the victim lines of an active cofactor. Thus, the active cofactor is effectively screened from a large number of interwire coupling noises, reducing the failures due to coupling noise dramatically.

In the experimental setup for measuring failures due to coupling noise, we randomly introduce coupling capacitors between 25%, per pair of nodes, both

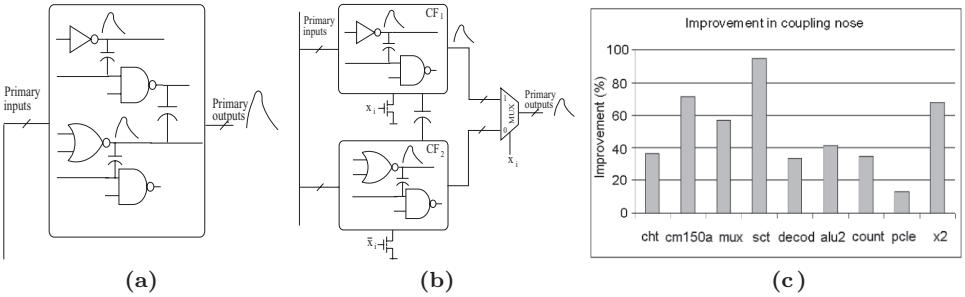

Fig. 1. (a) Noise propagation in original circuit, (b) Noise propagation after application of Shannon's expansion, (c) Improvement in coupling noise.

in ORG and SBS circuits. The values of capacitors are also randomly chosen between 0fF to 25fF. Next, an identical set of 500 random test patterns are applied to both the ORG and SBS circuits. A failure is registered if a signal transition fails to propagate to the output within a given delay bound. The simulation results are depicted in Figure 1(c). It can be observed that for all MCNC benchmark circuits, there is a drastic improvement in coupling induced failures. The average improvement in coupling noise in the proposed SBS approach is 50%. This is clearly due to the fact that the cofactor performing active computation is only affected by intra-cofactor coupling noise and coupling due to other cofactors are effectively eliminated.

7. LIMITATIONS OF SBS

The limitations of the proposed method are: (a) Shannon expansion requires modification of the synthesis flow; (b) it may result in increased area for multi-output logic circuits and may increase delay due to added multiplexers in some cases; (c) careful selection of control variable and number of expansions are required to minimize the area/delay overhead.

8. CONCLUSION

We have analyzed the testability of a circuit synthesized using the concepts of Shannon's expansion and supply gating. We demonstrate that modification in the synthesis process can result in circuits that consume lower power (both switching and leakage) but that are intrinsically more testable than designs produced by standard logic synthesis tools. We have shown significant improvement in four important aspects of testability. Existing DFT techniques to improve test length or power can be easily combined with SBS for further improvement.

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