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Defect Oriented Testing of Analog Circuits Using Wavelet Analysis of Dynamic Supply Current*,†

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Abstract. In recent years, Defect Oriented Testing (DOT) has been investigated as an alternative testing method for analog circuits. In this paper, we propose a wavelet transform based dynamic supply current (IDD) analysis technique for detecting catastrophic and parametric faults in analog circuits. Wavelet transform has the property of resolving events in both time and frequency domain simultaneously unlike Fourier transform which decomposes a signal in frequency components only. Simulation results on benchmark circuits show that wavelet transform has higher fault detection sensitivity than Fourier or time-domain methods and hence, can be considered very promising for defect oriented testing of analog circuits. Effectiveness of wavelet transform based DOT amidst process variation and measurement noise is studied.

Keywords: Defect Oriented Testing (DOT), dynamic supply current (IDD), Fourier transform, wavelet transform

1. Introduction

In recent years we have seen rapid evolution in analog and mixed-signal integrated circuits (ICs) in mobile and multimedia devices. This represents a relevant part of the market in production volume and applications. The integration of this type of circuits improves performance, cost and flexibility but complicates both the design and testing process. Analog and mixed-signal circuits have emerged more difficult to test than digital CMOS circuits and testing of the analog parts contribute significantly to the total manufacturing cost.

One important reason for the difficulty of analog testing is the effect of parametric variations which can cause the behavior of the fault-free device to deviate significantly from nominal values, masking the effect of the fault [16]. Cost of test increases in proportion to the precision required for testing with tolerance for parametric variations [14]. An efficient test method needs to be sensitive enough to precisely identify the deviations beyond the tolerance limit.

The slow and expensive nature of specification testing has motivated research into fault-based or structural test for analog circuits. Voltage measurement based techniques cannot access the internal nodes and has poor fault coverage for analog circuits. IDDQ testing in analog circuits have been explored because of its high fault coverage but it has problems like very high steady state currents in many analog circuits [3]. On the other hand, measurement of dynamic power supply currents has been found very useful for testing analog or mixed-signal ICs because of its potential to detect large class of manufacturing defects [9, 12, 17]. The current passing

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through the VDD or GND pin is measured under application of an input stimuli and the waveform is used to detect fault. While the waveform contains significant information about the circuit performance, appropriate analysis is required to extract specific knowledge about the signal. Existing analysis methods based on statistical or spectral properties of current waveform are effective for catastrophic faults but does not work well for parametric faults, which are more difficult to detect.

In this paper, we present a wavelet based dynamic current analysis method for fault detection in analog circuit. We show that wavelet decomposition has better sensitivity to detect parametric faults than techniques which use spectral or time domain information separately. Wavelet transform of a signal is a two-dimensional decomposition technique which analyzes the signal in multiple resolutions. Coefficients corresponding to each resolution localize events in time domain. Hence, wavelet transform coefficients of a signal contains both time and frequency information making it more suitable for fault detection. In our work, we have used a simple metric for comparing the sensitivity of the wavelet method with DFT based method and a time domain method. Simulation results on two benchmark circuits demonstrate the superiority of wavelet method for parametric faults.

The rest of the paper is organized as follows. Section 2 describes previous work on supply current testing of analog circuits. Section 3 presents basic ideas about wavelet transform. Section 4 deals with fault detection using wavelet transform of the IDD signal. In Section 5 we present the simulation results. In Section 6, we consider some important issues for analog fault detection using wavelet. Section 7 concludes the paper.

2. Previous Work on IDD Testing for Analog Circuits

Some of the initial work on IDD testing was done by Frenzel and Marinos [11] in 1987. They investigated a small TTL and described the complete power supply current as a signature of the Device Under Test (DUT). Camplin et al. [9] explored the suitability of supply current monitoring as a unified technique for the testing of analog and digital portions of Mixed ASICs. They used the absolute value of the supply current level for different set of input stimuli as signature.

Gielen et al. [12] presented a new method for testing both DC and AC faults in analog circuits. Time domain testing followed by DFT based spectral analysis is applied to detect faults. Beasley et al. [4] investigated an IDD pulse response testing by pulsing the power rails and analyzing temporal and/or spectral characteristics of the transient current. Graeb et al. [17] use process specific (parameter statistics) and circuit specific (performance specification) fault model. They used DFT based signature comparison to detect faults.

Spinks [22] dealt with the issue of process parameter variation and the choice of correct stimulus for optimum fault coverage in analog circuits. They chose the best test stimuli using sensitivity analysis and then produced the test margin by fault simulation considering process variation. It is directed specifically to detect *hard* faults using RMS (Root Mean Square) supply current monitoring. Somayajula et al. [21] used fault dictionary based approach to detect fault but applied ramp input to obtain better fault coverage. Kilic and Zwolinski [16] used both the RMS value of the AC supply current as well as the DC current level to detect faults in analog circuits. They varied the supply voltage at fixed steps to improve fault coverage.

While supply current analysis has been well-studied for fault detection in analog circuits, an efficient current analysis technique, which works well for parametric faults in presence of measurement noise and process variation, is not established. Appropriateness of using wavelet analysis for fault diagnosis in analog circuits using neural network has been explored in [1]. The authors in [1], use wavelet transform for preprocessing the impulse response of a analog circuit to extract distinctive features across fault classes. Wavelet-based supply current analysis has been explored as an effective test techniques alternative or supplementary to static current testing (IDDQ) in digital circuits [7, 20]. Efficiency of wavelet analysis for fault detection in analog circuits has been investigated in [6] and compared to other supply current testing methods. In this paper, we have investigated the potential of wavelet transform as a supply current analysis technique for defect based testing of analog circuits with high detectability of faults under background noise.

3. An Overview of Wavelet Transform

Wavelet transform is a mathematical operation that decomposes input signal simultaneously into time and

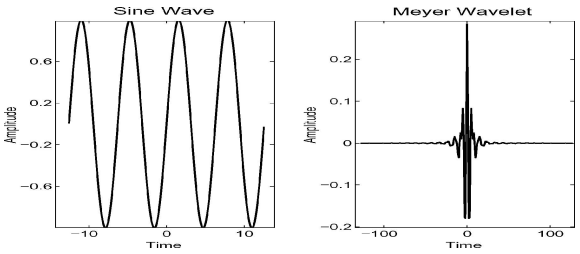

Fig. 1. Basis functions for Fourier (sinewave) and wavelet (meyer) transforms.

frequency components [8, 10, 19]. Fourier analysis has a serious drawback since it transforms signal in frequency domain and hence, it is not possible to localize an event in time scale just by looking into the Fourier coefficients of a signal. Wavelet decomposition of a signal, on the other hand, can resolve events in both time and frequency domain, which turns out to be very useful in fault detection. In wavelet transform we take a real/complex valued continuous time function with two properties—(a) it will integrate to zero, (b) it is square integrable. This function is called the *mother wavelet* or wavelet. (This has to satisfy another property called *admissibility*, to perform the inverse transform). Property (a) is suggestive of a function which is oscillatory or has wavy appearance and thus in contrast to a sinusoidal function, it is a small wave or wavelet (Fig. 1). Property (b) implies that most of the energy of the wave is confined to a finite interval.

The CWT or the Continuous Wavelet Transform of a function $f(t)$ with respect to a wavelet $\Psi(t)$ is defined as:

$$W(a,b) = \int_{-\infty}^{\infty} f(t)\Psi^*_{a,b}(t)\,dt \tag{1}$$

$$\text{where } \Psi_{a,b}(t) = \frac{1}{\sqrt{|a|}}\Psi\left(\frac{t-b}{a}\right) \tag{2}$$

Here a, b are real and $*$ indicates complex conjugate. $W(a,b)$ is the transform coefficient of $f(t)$ for given a, b. Thus the wavelet transform is a function of two variables. For a given a, $\Psi_{a,b}(t)$ is a shift of $\Psi_{a,0}(t)$ by an amount b along time axis. The variable b represents time shift or translation. Since a determines the amount of time-scaling or dilation, it is referred to as *scale* or dilation variable. If $a > 1$, there is stretching of $\Psi(t)$ along the time axis whereas if $0 < a < 1$ there is a contraction of $\Psi(t)$ (Fig. 2). Each wavelet coefficient $W(a,b)$ is the measure of approximation of the input waveform in terms of the translated and dilated versions of the *mother wavelet*. Fig. 1 compares the basis signals of DFT and wavelet transform. The *mother wavelet* shown in Fig. 1 is called *meyer* wavelet. Fig. 2 shows a translated and dilated *mother wavelet* (Mexican hat) used to approximate an IDD waveform of an mixed-signal circuit. Fig. 3 shows the wavelet components of the IDD signal in Fig. 2 at four different *scales*. It can be noted that components have rapidly diminishing magnitudes at higher frequencies

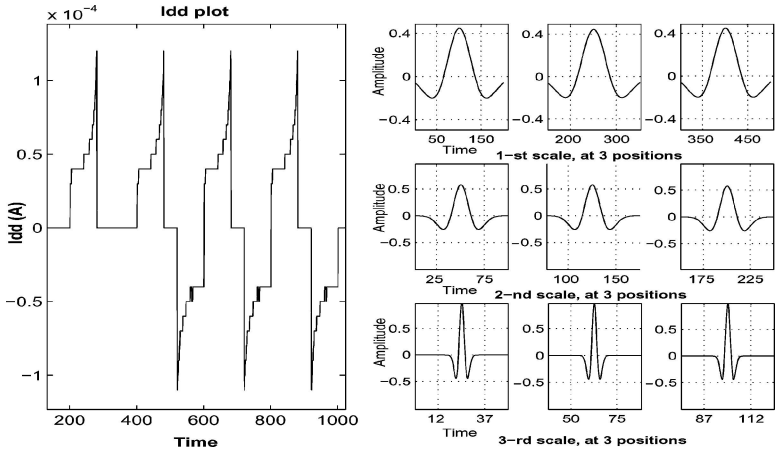

Fig. 2. IDD waveform from a digital to analog converter with parametric fault (left) and *mother wavelet* (Mexican hat) at different *scale*s and positions used in wavelet transform.

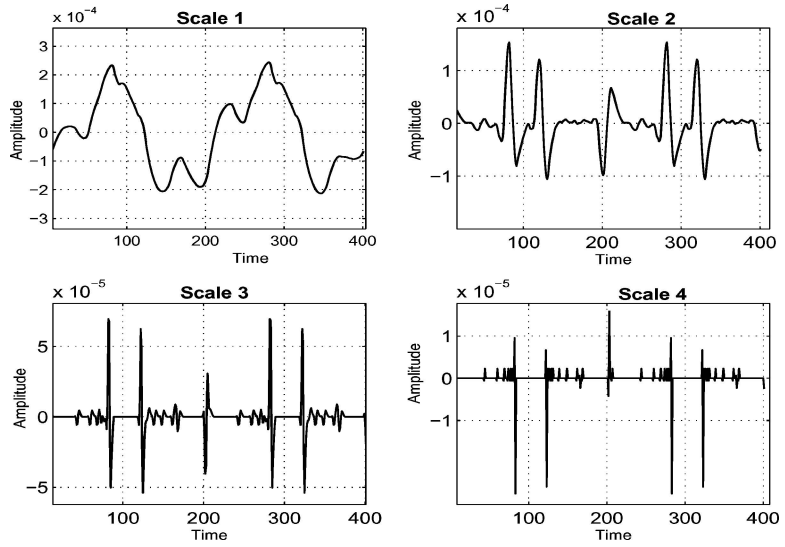

Fig. 3. Wavelet coefficients at different *scale*s obtained from current waveform in Fig. 2.

(higher *scale*s). Two important properties of the basis wavelet, that determines how efficiently it can represent the original signal, are (a) regularity and (b) support. The regularity gives a measure of the smoothness of the wavelet function with higher regularity implying a smoother wavelet, while the support measures the effective width of the wavelet function in time domain [8, 10].

4. Fault Detection Using Wavelet Transform

Fig. 4 plots dynamic supply current responses for a fault-free and faulty (parametric fault) analog filter with their corresponding DFTs. Fig. 5 plots the wavelet components of these responses at two different *scale*s. It can be observed that wavelet components capture more variation in their value (mainly ins the first scale) than DFT and they represent the variation in the IDD waveform better than DFT. The proposed wavelet based fault detection process is similar to existing Root Mean Square (RMS) error measurement technique that uses the dynamic current of the circuit [23]. Dynamic supply current of an analog circuit is observed in response to a transient input stimuli. The sampling rate should depend on the specific precision required and frequency content of the response. Current waveform is then subjected to wavelet transform to generate a two dimensional set of coefficients. In case of wavelet decomposition, we need to choose an appropriate basis function (*mother wavelet*) unlike DFT, which has a fixed basis.

The two dimensional set of wavelet coefficients obtained from a test circuit (DUT) for a particular input stimuli, is then compared with those from a golden circuit for the same stimuli. We compute the RMS error between the coefficients for comparing the response of the DUT with golden circuit. An RMS error which is more than a pre-determined test margin indicates a faulty DUT. The precision of the testing process depends on the quality of the test margin. Manufacturing process parameter variations and measurement hardware noise need to be taken into account in identifying test margin. In addition, the success of the test largely depends on the choice of input stimulus which plays important role in determining fault coverage [22].

In this research, our primary goal is to show wavelet transform as a more efficient dynamic current waveform analysis than DFT and other supply current analysis based DOT methods [12, 16] for detecting faults in analog circuits. We have chosen a simple RMS error metric for comparing the sensitivity of the wavelet based testing with DFT or time-domain method. The reason for choosing RMS metric over others is its simplicity and wide popularity. In the following equations G_i's are the coefficients for golden circuit response and F_i's are those for DUT response. Equation (3) represents the RMS value of difference. The normalized

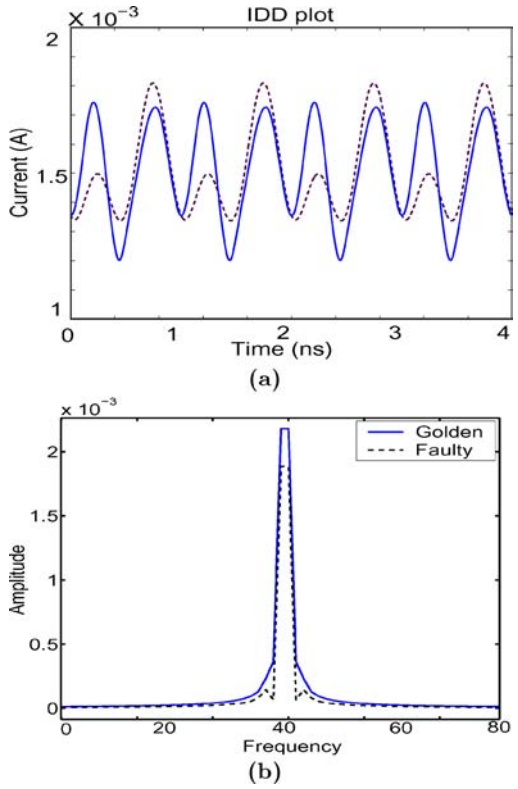

Fig. 4. IDD (a) and DFT (b) plot for a faulty response (parametric fault) of an analog filter.

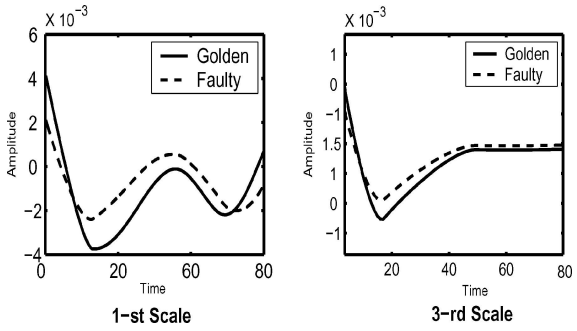

Fig. 5. Corresponding wavelet components at two different scales.

RMS, as in Eq. (4) can be considered a direct measure of the sensitivity of the transforms. In Eq. (4), we use the fault free components (G_i) for normalization. It computes the root mean square value of the difference as a fraction of the corresponding golden circuit coefficient (G_i). In addition to DFT method, we also use a pure time domain approach based on charge computation (area under supply current curve) to compare the wavelet method.

$$RMS = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(F_i - G_i)^2} \tag{3}$$

$$normRMS = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(\frac{F_i - G_i}{G_i}\right)^2} \tag{4}$$

5. Simulation Results

To compare the effectiveness of wavelet transform based fault detection with existing analysis techniques, we applied the methods on two benchmark circuits and observed their performance using sensitivity metric mentioned earlier. One of the circuits is a leapfrog filter (Fig. 6) and the other is a continuous-time state-variable filter (Fig. 7). Both are taken from the ITC'97 set of benchmarks [15]. We have used the TSMC 250 nm node of technology with the corresponding model files. We have scaled the ITC benchmark netlists to the

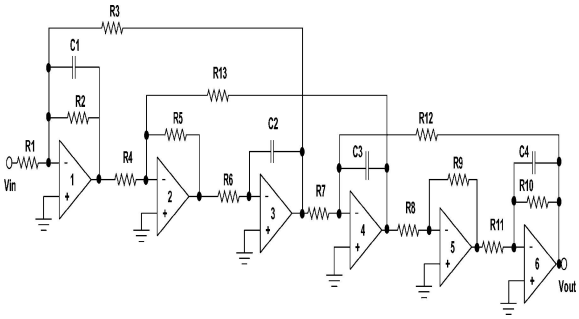

Fig. 6. Analog benchmark circuit: leapfrog filter (*ITC'97*).

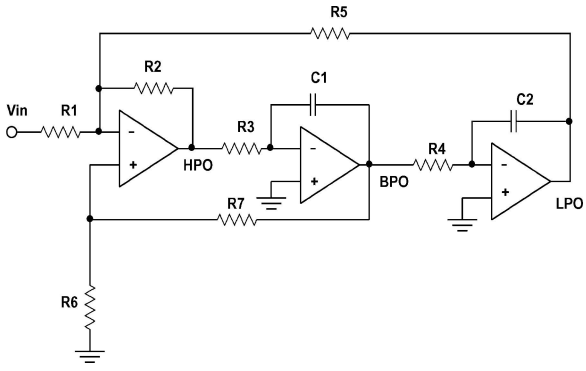

Fig. 7. Analog benchmark circuit: continuous-time state-variable filter (*ITC'97*).

Table 1. Comparison of sensitivity for parametric faults.

Design	Fault	RMS(Wav)	RMS(DFT)	ERRQ	*NormRMS*(Wav)	*NormRMS*(DFT)	NormQ
LF	C4, +6s	525962.0	627369.9	575.2	1.86	0.24	0.11
	C2, −6s	1179645.0	969349.8	869.3	7.41	0.45	0.17
	R1, −6s	3809144.3	6193127.5	2456.5	3.68	0.61	0.47
	R2, −6s	2190771.0	3554285.6	1845.3	2.74	0.51	0.35
	Vt, +10%	248464.0	402469.6	626.5	0.24	0.04	0.12
CTSV	C1, −6s	2094.3	1422.6	33.1	27.57	0.40	0.10
	C1, +6s	1465.9	976.9	27.1	15.26	0.23	0.08
	C2, +6s	836.9	607.4	20.3	7.30	0.17	0.06
	R7, +6s	2417.0	2937.7	40.5	4.10	1.22	0.12
	R5, +6s	9954.8	11362.3	100.1	32.10	1.67	0.30

250 nm TSMC technology node from the original description of the benchmarks in Mitel Semiconductor's 1.2u and 1.5u technology [15]. We performed simulations on the *Hspice* netlists of the circuits with AC input stimuli for both circuits.

We have chosen sinusoidal waveforms for input stimulus to our filters. The frequencies of the sinusoids are equal to the pole frequencies of the filters. This is because at that frequency, the filter transfer function undergoes a sharp change in magnitude as well as phase and hence any deviation from the ideal gets well reflected in the dynamic supply current [5]. The sampling frequency used for both circuits is 5 GHz.

The *mother wavelet* chosen was *db2* [10]. We used Matlab software for computing the DFT and wavelet coefficients. To model catastrophic faults we used a bridging resistance of 10 Ω for shorts. Opens were modeled using a 100 MΩ resistance. Parametric faults were modeled either by $\pm 6\sigma$ variation in circuit component or by varying the transistor threshold voltage (Vth). The σ value of component variation is determined in such a way that the component is allowed to vary up to 3σ, yet the analog circuit will meet its specification. We chose as a default system specification, a maximum deviation of 10% in gain and phase response from the corresponding response of the circuit with nominal values for the components. We used the same number of frequency components for both wavelet and DFT methods (starting from the DC value). Coefficients with very small value were not considered to compute the normalized error. The scales in wavelet transform were dyadic (power of 2) starting from 8 to 64. In DFT-based method, we consider both magnitude and angle (phase) components of a coefficient for computing *normRMS*. For *normRMS* of charge, we take the absolute difference in area under IDD curve (obtained from numerical integration) normalized to the area for the non-faulty case.

Table 1 shows the result of comparison for parametric faults in both circuits. 'LF' stands for circuit leapfrog filter and 'CTSV' for continuous-time state-variable filter. Column 2 specifies the kind of parametric fault introduced in the circuit. Column 3 and 4 are the RMS error for wavelet and DFT method respectively. Column 5 (ERRQ) is the error calculated as difference in area under current waveform, while the column 6, 7 and 8 represent the normalized error value for all three cases. It can be observed that the wavelet based method has significantly better sensitivity than the other two methods. The average sensitivity for wavelet is about 25 times of DFT and about 80 times of the charge based method (NormQ) for the 10 parametric faults considered in Table 1.

The test margin for the catastrophic faults should fall outside the test margin required to detect the parametric faults. To verify that it is true for wavelet based testing, we experimented with a set of catastrophic faults in the leapfrog filter and computed the sensitivity. Table 2 shows that catastrophic faults can be detected using the test margin for parametric faults and wavelet based method has the better sensitivity measure also for the catastrophic faults.

Since all resistive short and open defects may not lead to catastrophic faults, we have studied the fault detection capability of the proposed scheme for different bridging resistances. As can be shown from Table 3, the sensitivity of detection goes down with increasing

Table 2. Comparison of sensitivity for catastrophic faults for the leapfrog filter in Fig. 6.

Fault	RMS(Wav)	RMS(DFT)	ERRQ	NormRMS(Wav)	NormRMS(DFT)	NormQ
R8, VCC bridge	59724930.8	83412522.5	8936.2	142.61	10.21	1.69
C2 shorted	16354037.4	26511764.3	5075.5	15.73	2.72	0.96
Drn/Src short, Opamp4, NMOS M3	14492540.8	21761478.2	4571.2	51.36	2.04	0.87
R5 Open	27378158.7	28496386.6	4910.6	1228.67	11.74	0.93
Drn/Gate short, opamp5, PMOS M7	7173998.5	10345002.0	3135.3	22.44	1.41	0.59

Table 3. Comparison of sensitivity for bridging faults.

		Bridging resistance				
Design	Fault	10 Meg	1 Meg	10K	1 K	100 Ω
LF	R8, VCC bridge	0.02	0.9	20	65	130
	R5 open	1228.12	1226.6	800.02	204.67	115
	C2 short	0.01	0.02	1.09	2.4	15.73
CTSV	Drn/Src short in OPAMP 2	0.3	2.1	12.4	15.1	21.22
	Input of OPAMP, VDD bridge	0.01	23.4	327.923	876.43	1742.8
	R3 open	529.33	213	56.99	12	0.45

Table 4. Equivalent no of components in DFT for iso-sensitivity.

Design	Fault	No. of coefs (Wav)	No. of coefs(DFT)/ (total coefs)
LF	C4, −6s	4	74 (74)
	R5 open	4	59 (74)
	C3, +6s	4	74 (74)
	Vth, 10%	4	74 (74)
CTSV	C2 +6s	4	80 (80)
	R5, +6s	4	43 (80)
	R7, −6s	4	75 (80)
	R6, +6s	4	70 (80)

(decreasing) values of resistances for resistive shorts (opens).

For Tables 1 and 2 the number of frequency components used is 8 starting from the lowest frequency component for both wavelet and DFT methods. It is observed that the DFT coefficients converge to zero at a very slow rate and we can get equivalent sensitivity in DFT method only if we consider large number of frequency components. Table 4 presents the number of frequency components for DFT, that is required to have normalized RMS equivalent to that in wavelet using 4 frequency components. The observation supports a salient property of wavelet transform that, for a reasonably good basis function, wavelet can represent a signal with high accuracy in fewer terms than DFT.

Fig. 8 plots the fault coverage of two methods to compare their effectiveness to detect fault for a fixed normalized error. We considered a total of 23 parametric and 5 catastrophic faults in two test circuits. The plot shows that for a Normalized RMS error of 0.25 we can detect 1.6 times more faults using wavelet while it is 5.8 times for an error bound of 5. The plot in Fig. 9 compares the distribution of normalized RMS for two cases. For this plot we considered 10 parametric faults as in Table 1. It can be noted that the error distribution for wavelet has more deviations across faults than DFT.

6. Test Design Issues

6.1. *Impact of Power-Grid*

Analog circuits has a much simpler power-grid than its digital counterpart, which gives them an inherent advantage for current based testing. In digital circuits,

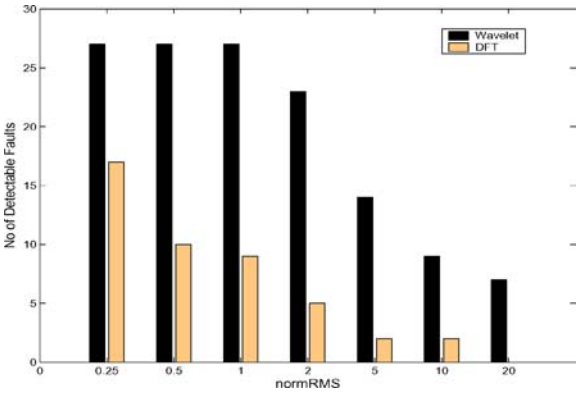

Fig. 8. Comparison of fault coverage for wavelet and DFT method.

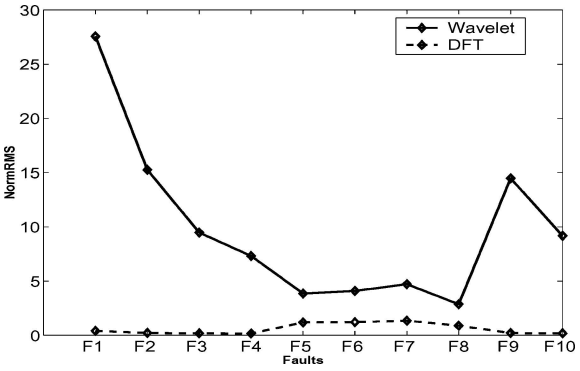

Fig. 9. Distribution of normalized RMS for 10 different faults.

power-grids usually have very complex topology with significantly larger number of transistors connected to it than in analog circuits. Furthermore, digital circuits usually require placement of more decoupling capacitances in their power-grid than analog circuits to reduce supply noise. Hence, the impact of a defect in the supply current is less noticeable in digital circuits. Application of current based testing in case of digital circuits, therefore, need circuit partitioning or proper test vector selection to improve the defect sensitivity. On the other hand, analog power-grid has much less impact on supply current due to its simpler topology and impact of defect on the current is not masked by the power supply network.

6.2. *Choice of Mother Wavelet*

Mother wavelets are orthogonal basis systems with a wide variety of functional properties from smooth to very irregular. Selection of basis for wavelet analysis (*mother wavelet*) has impact on the sensitivity of fault detection. This is observed in Table 5. In this table, we list the RMS and normalized error value for two different faults using different *mother wavelet*s. For the test circuit (leapfrog filter) and the faults considered, we can observe that the basis *Meyer* wavelet has the best sensitivity while the Mexican hat *Mexhat* wavelet has the least. One significant advantage of using wavelet for fault detection is that we can choose the basis wavelet according to application i.e. in this case, we can choose the basis function, which fits to the IDD waveform of the golden circuit best. Among the mother wavelets we have examined, orthogonal wavelets with compact support like *Meyer* and *db2* usually give very good mean square error, since they closely match with the supply current waveform.

Table 5. Variation in sensitivity with different mother wavelets.

Fault	Mother wavelet	*RMS*	*NormRMS*
C1, +6s	Db2	1829709	6.654
	Meyer	1642714	31.739
	Mexhat	2104196	5.082
	Haar	1784817	11.198
R4, −6s	Db2	333998	2.083
	Meyer	316531	16.164
	Mexhat	398779	1.260
	Haar	322134	2.344

6.3. *Increasing Fault Coverage by Supply Voltage Variation*

For analog circuits, the fault coverage of the supply current testing methods can be improved if it is possible to switch transistors between different regions of operations. Variation of supply voltage is an approach by which we can achieve some control over the behavior of the transistors, thereby increasing the fault coverage. Kilic et al. [16] and Somayajula et al. [21] have proposed two different strategies of supply current variation for better testability. We experimented with varying supply voltage to investigate the effectiveness of wavelet method under these circumstances. In Table 6, we present the sensitivity of the two current testing methods for several catastrophic faults when a ramp input is applied to the supply rails for the leapfrog filter. We consider only first 8 frequency components

Table 6. Sensitivity measure for ramp input in supply rails.

Faults	*RMS* (Wav)	*RMS* (DFT)	*NRMS* (Wav)	*NRMS* (DFT)
R6, VEE bridge	23.12	38.85	6.601	1.283
PMOS M1 GOS (opamp4)	36.07	60.76	10.44	2.00
PMOS M7 GOS (opamp5)	26.47	44.13	7.529	1.216
Rc open, opamp3	21.15	1.91	1.05	0.06
R8, VCC short	2322.33	139.12	23.34	4.39

for both the cases. The result demonstrates that for current testing schemes which use supply voltage variation for better fault coverage, wavelet is about 7 times more sensitive than DFT.

6.4. *Performing Wavelet Analysis*

Once the dynamic supply current waveform is sampled and quantized, we need to perform wavelet transform on it. This can be done either in software running on a general purpose processor or digital signal processing engine, or dedicated hardware optimized to perform wavelet transform efficiently. Computational complexity of a discrete wavelet transform (DWT) is $O(n)$, whereas it is typically $O(n)\log(n)$ for DFT with n data samples [13]. One of the main contributions of wavelet theory is to relate discrete-time filter banks with continuous time function space. In the discrete case, filters of different cut-off frequencies are used to analyze the signals at different scales. The scale is changed by upsampling and downsampling operations [8]. Since wavelet is being increasingly used in image and video analysis due to its very good decorrelation property, efficient algorithms for wavelet transform has been developed for real-time signal processing. Hence, a software-based wavelet analysis platform of the supply current signal can be an effective solution.

There are, however, number of emerging VLSI architecture for hardware implementation of the wavelet transform algorithm. These implementations, similar to implementation of DFT, use a discrete-time filter banks and employ either a serial or a parallel architecture (depending on how the inputs are supplied to the filters). The architectures interleave computation of outputs of different levels and use pipelining to reduce storage and latency. Recently, lift-based forward and reverse wavelet transform has been proposed which requires far fewer computations and significantly less memory than convolution-based DWT [2]. The proposed implementations of wavelet transform have similar processing speed and hardware overhead as implementation of discrete Fourier transform [2, 13].

6.5. *Impact of Sampling Frequency and Measurement Noise*

Effect of measurement hardware error is an important factor to consider for fault detection especially for off-chip supply current monitoring [17]. Usually the measurement hardware acts as a low pass filter smoothening out many high frequency components. Hence, the detection technique which largely depends on the high frequency components, is not suitable for off-chip testing. In our experiments, we have shown that wavelet renders a more sensitive detection method than DFT when both use only lower frequency components of IDD for fault detection. This observation makes wavelet a more promising technique than DFT for off-chip testing.

For computation of wavelet or DFT of the dynamic supply current waveform, an ADC (analog to digital converter) followed by a digital signal processing unit should be used. Hence, the resolution of the mean square error will depend, along with the precision of wavelet transform, on the sampling frequency as well as the number of bits used to quantize the sampled waveform. The effect of sampling frequency on the RMS error has been shown in Table 7. It can be noted that

Table 7. Comparison of detection sensitivity at different sampling frequency.

		NormRMS error at sampling frequency (Hz)			
Design	Fault	5.00E+09	1.00E+09	8.00E+08	5.00E+08
LF	C4, +6s	1.86	1.8	1.1	0.21
	C2, −6s	7.41	4.5	4.2	0.5
	R1, −6s	3.68	3.7	2.8	0.09
	R2, -6s	2.74	1.5	0.7	0.08
	Vt, +10%	0.24	0.18	0.05	0.06
CTSV	C1, −6s	27.57	15.4	4.09	0.8
	C1, +6s	15.26	7.4	2.2	0.7
	C2, +6s	7.3	2.5	1.03	0.08
	R7, +6s	4.1	1.2	0.9	0.02
	R5, +6s	32.1	33	19	0.9

Table 8. Comparison of sensitivity for different quantization.

Design	Fault	*normRMS* with 16-bit quantizer	*normRMS* with 8-bit quantizer	% Error from 16-bit	*normRMS* with 4-bit quantizer	% Error from 16-bit
LF	C4, +6s	1.860	1.860	0	1.900	−2.105
	C2, −6s	7.410	7.420	−0.135	7.200	2.917
	R1, −6s	3.680	3.670	0.272	4.100	−10.244
	R2, −6s	2.740	2.740	0	2.600	5.385
	Vt, +10%	0.240	0.240	0.000	0.180	33.333
CTSV	C1, −6s	27.570	27.570	0	28.500	−3.263
	C1, +6s	15.260	15.260	0	14.000	9.000
	C2, +6s	7.300	7.300	0	7.100	2.817
	R7, +6s	4.100	4.100	0	5.000	−18.000
	R5, +6s	32.100	32.100	0	28.200	13.830

decreasing sampling frequency reduces the RMS error between the golden and faulty supply current waveforms, thereby decreasing fault coverage.

Table 8 shows the effect of quantization noise on the RMS error for different parametric faults. Quantization noise is determined by the number of bits used for digital signal processing. It can be observed that the RMS error between the golden and faulty waveforms decreases as the quantization noise increases. However, both 16-bit as well as 8-bit sampled values give reasonable accuracy for fault detection. The effectiveness of fault detection goes down significantly if a 4-bit quantizer is used.

6.6. Process Variation

Dynamic supply current testing, like other defect based testing methods for analog circuits, is an indirect test method in the sense that it does not check the circuit behavior or specifications directly. Hence, one of the important criteria to judge the effectiveness of supply current testing would be to study how the method performs under process variation. Transistor parameters and component values shift due to process fluctuation causing significant variation in the shape and magnitude of supply current. It is a challenging task to determine the test margin considering process variation in such a way, that impact of genuine defects is not masked and at the same time, yield is not affected.

Specification-based testing of analog circuits is capable of detecting both catastrophic and parametric faults. However, in addition to being expensive with respect to test cost and time, it is often quite difficult and at times impossible to do specification-based testing of each individual blocks in a mixed-signal circuit separately. The outputs of certain blocks, for example the outputs of a filter, may not be available for off-chip measurement. If the output of a filter is taken to a pin, then the pin capacitance often introduces distortion and performance degradation, which may not be within the limits of tolerance. Such cases typically arise in mixed-signal circuit design. Hence, the method developed in our paper is useful because it can detect catastrophic faults from the dynamic supply current measurement at the VDD pin.

To check how wavelet based supply current testing perform in comparison with other two supply current test methods considered, we performed some experiments with a 2-nd order 1-bit sigma-delta ADC as described in Fig. 10 [18]. We determined 25 different process points with varying transistor threshold (both nMOS and pMOS) and component values in the range of $\pm 10\%$. We used the normalized RMS value of difference as the test metric and the maximum *normRMS* computed for the 25 process points was taken as the test margin. Then we injected 25 different catastrophic faults at arbitrary locations in the circuits and tested the circuit for these faults in all the three methods. For different process corners and catastrophic faults in different simulations runs, scatter plots have been generated for the RMS error. The test margin for pass/fail decision is so selected that process variation is tolerated while ensuring that the maximum number of faults are detectable. Fig. 11 (a)–(c) represent

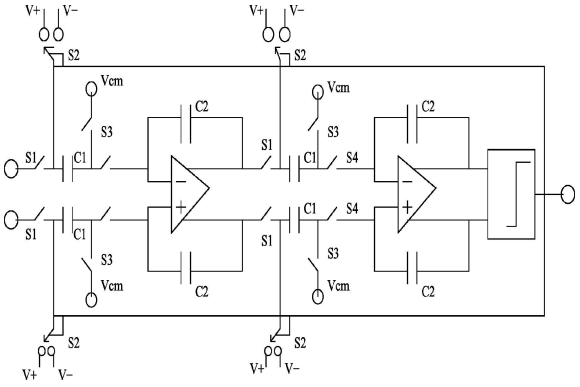

Fig. 10. Schematic of a 2-nd order 1-bit sigma-delta ADC.

the scatter plots for wavelet, DFT and charge based methods respectively, which shows *normRMS* for different process points and catastrophic faults. Fig. 12 presents a bar plot for the test results, which shows that with different test margins in the three different methods, wavelet transform based testing has better defect coverage than the other two methods. Hence, wavelet transform can be an effective solution for testing defects in analog circuits in the presence of process variation.

7. Conclusion

Wavelet decomposition based dynamic supply current analysis has been shown to have better sensitivity than pure DFT or time-domain analysis method. This can be attributed to the property of wavelet transform to decompose the IDD signal in multiple resolutions keeping the timing information in place. Better sensitivity can help us get better fault coverage than pure spectral analysis for detecting parametric faults. Wavelet is particularly useful for off-chip analysis of IDD, because high frequency components of the current are usually filtered out by the measurement hardware and wavelet can approximate the residue signal better than DFT. Another important advantage of using wavelet over DFT is that we can use the *mother wavelet* to adapt to the current waveform of the particular circuit, producing better representation of the signal in terms of transform components. This is not possible with Fourier transform which has a fixed sinusoidal basis function.

Wavelet can be used for specification based testing as well. We believe, specification of an analog circuit

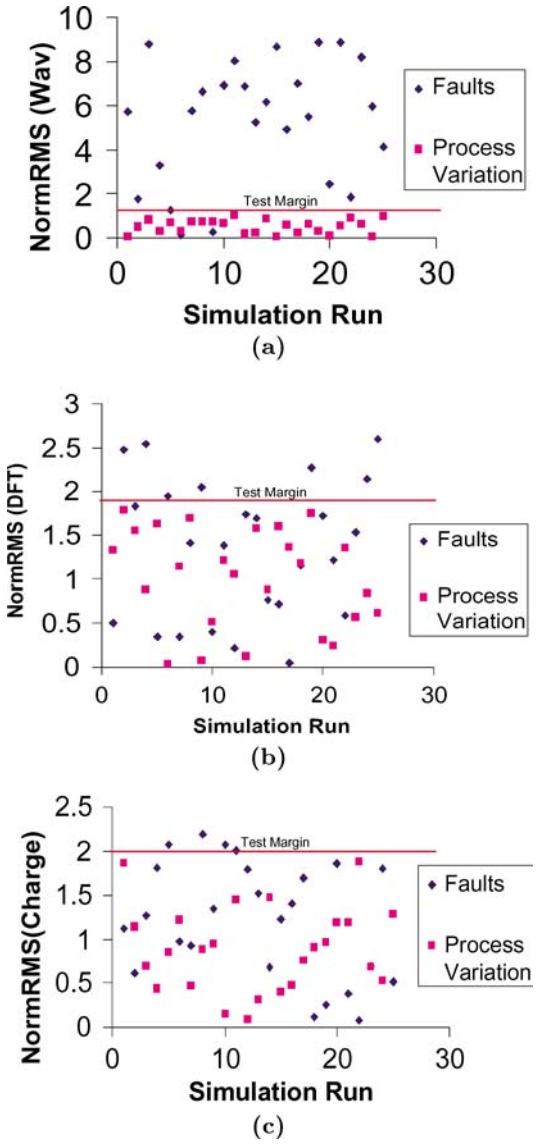

Fig. 11. Detection of test margin under process variation for the three methods.

e.g. the gain-bandwidth product can be better modeled by wavelet components because wavelet can better represent measured signal than DFT. Our research has also shown [7] that wavelet is very promising for fault detection in digital CMOS circuits. This makes it a suitable candidate for testing Mixed-signal circuits with a unified testing solution for both digital and analog parts. Since wavelet can resolve events in time and frequency domain simultaneously, we can possibly use the timing information for fault localization.

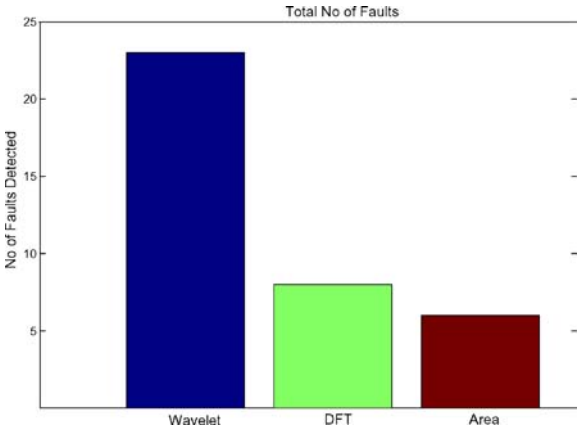

Fig. 12. Comparison of fault coverage in three methods in the presence of process variation.

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