Exploring Spin Transfer Torque Devices for Unconventional Computing

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(Invited Paper)

***Abstract*—This paper reviews the potential of spin-transfer torque devices as an alternative to complementary metal–oxide–semiconductor for non-von Neumann and non-Boolean computing. Recent experiments on spin-transfer torque devices have demonstrated high-speed magnetization switching of nanoscale magnets with small current densities. Coupled with other properties, such as nonvolatility, zero leakage current, high integration density, we discuss that the spin-transfer torque devices can be inherently suitable for some unconventional computing models for information processing. We review several spintronic devices in which magnetization can be manipulated by current induced spin transfer torque and explore their applications in neuromorphic computing and reconfigurable memory-based computing.**

***Index Terms*—Domain wall motion, in-memory computing, magnetic tunnel junction, neuromorphic computing, spin torque oscillator, spin transfer torque.**

I. Introduction

With Dennard scaling of complementary metal–oxide–semiconductor (CMOS) devices slowing down, work has started to explore new devices that can potentially replace CMOS. Although extensive research for the "next switch" has not yet yielded a clear winner, many of the new devices that have been explored, such as the spin-transfer torque devices [1]–[7] or the tunnel field-effect transistors [8], [9], have unique characteristics that set them apart from traditional MOS transistors. To truly leverage the potential of these devices, there is a need to explore new computing models that are uniquely suited to the characteristics of these devices, thereby attaining performance that CMOS cannot achieve. Recent experiments on spintronic devices have demonstrated high speed switching of nano-scale magnets with spin polarized currents [4], [5]. Together with other characteristics, including nonvolatility, zero current leakage and high integration density, spin-transfer torque devices have been explored to design compact, high-speed, low-power memory and Boolean logic [28], [34], [72]. While the suitability of spin-transfer torque (STT) devices for on-chip memory is widely accepted, the suitability of spin-torque devices for logic applications is debatable [72]. However, a wider perspective on the application of spin-transfer torque devices would involve exploring combination of spin and charge devices and searching for computation models enabled by their unique capabilities to truly leverage their benefits. In this paper, we review several spintronic devices in which magnetization can be manipulated by the current induced spin transfer torque and explore the applications of these devices in unconventional computing, including neuromorphic computing and reconfigurable in-memory computing.

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II. Spin Transfer Torque Effect and Devices

In this section we present the basics of the STT phenomenon and review device structures that can be attractive for many applications such as recognition, matching, using brain-inspired computing models [39]–[41]. The storage devices can also lead to new energy-efficient computing fabrics, such as reconfigurable memory-based computing [43], [73]. The ability to realize both logic and random access memory block (STTRAM) [78]–[80] using STT devices can enable in-memory computing inside last level memory of a computer system to accelerate diverse data-intensive kernels. Benefits of such in-memory computing has been recently studied in the context of flash memory [74], [75]. The random access capability and lower power access of STTRAM is highly promising for future-generation in-memory computing platforms.

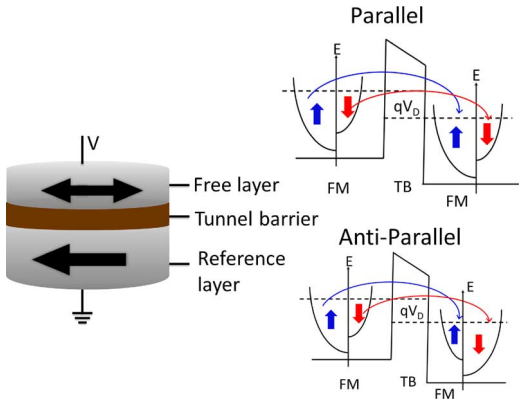

Fig. 1. Physical structure of MTJ and its band structure of parallel and anti-parallel configurations.

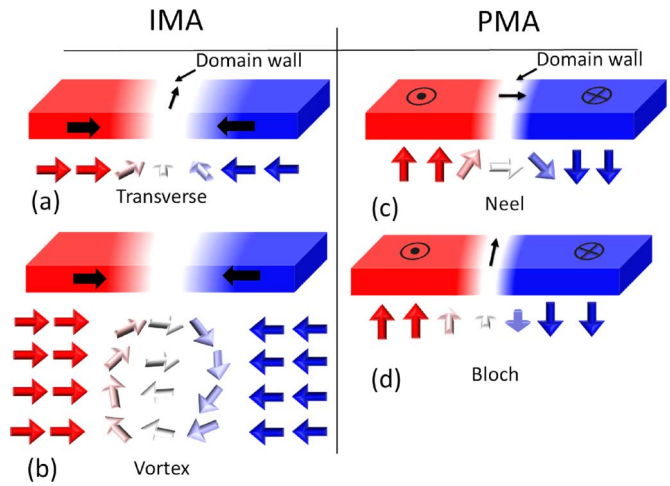

Fig. 2. Typical domain wall structure (a) in-plane magnetic anisotropy transverse head-to-head transverse DW, (b) IMA vortex DW, (c) perpendicular magnetic anisotropy nanowire with Neel DW, and (d) PMA Bloch DW.

A. Magnetic Tunnel Junction

The typical magnetic tunnel junction (MTJ) structure is shown in Fig. 1. It consists of two ferromagnetic layers with a tunnel barrier sandwiched between them [6], [10]–[12]. One of the layers is a fixed magnetic layer, while the other one is a free magnetic layer. The key characteristics of the MTJ arise from the fact that the ferromagnetic layers act as polarizers of electron spin, which is illustrated by the band diagrams in Fig. 1. As a result, the tunneling probability of electrons across the tunnel barrier depends on the relative magnetization directions of the pinned and free magnetic layers which manifests as the tunneling magneto-resistance (TMR) effect [6], [10]–[12]. Hence, electrons flowing through the MTJ are spin polarized, and the band structure of the stack introduces a *spin filtering effect*.

As Fig. 1 shows, electrons can only tunnel into the subband of the same spin orientation in the absence of spin-flip processes. When the magnetization directions of the ferromagnetic layers are *parallel* (P), the number of filled and empty electronic states (for each spin) are well matched. On the other hand, the same electronic states (for each spin) are mismatched when the magnetization directions of the ferromagnetic layers are *anti-parallel* (AP). Thus, the tunneling conductance of the MTJ is high (low) when the MTJ configuration is P (AP). Furthermore, the tunneling conductance of the MTJ can be expressed as

$$G(\theta) = \frac{1}{2}(G_P + G_{\mathrm{AP}}) + \frac{1}{2}(G_P - G_{\mathrm{AP}})\cos\theta \qquad (1)$$

where θ is the relative angle of two ferromagnetic layer magnetization orientations, GAP and GP are the conductance when $\theta = 180^\circ$ (two magnetization orientations are anti-parallel) and $\theta = 0^\circ$ (two magnetization orientations are parallel), respectively. We may then define the TMR ratio, which quantifies the distinguishability between P and AP states of the MTJ, as

$$\mathrm{TMR\ ratio} = \frac{G_P - G_{\mathrm{AP}}}{G_{\mathrm{AP}}}. \qquad (2)$$

Since the spins of electrons flowing through the MTJ are polarized, they exert spin-transfer torque (STT) on the magnetization of the ferromagnetic layers. The magnetization of the fixed layer is strongly pinned so that STT acting on it is negligible. When electrons enter a nano-magnet, the electrons experience an exchange field that tries to align their spin directions with the magnetization direction of the nano-magnet. Thus, the electrons experience a torque in the magnetization direction of the nano-magnet. Due to angular momentum conservation, an equal and opposite torque is exerted on the magnetization of the nano-magnet. This torque arises due to exchange of spin angular momentum between electrons and nano-magnet, and is called *spin-transfer torque*. Thus, spin-polarized electrons flowing through the MTJ exert STT that rotates the magnetization of the free layer parallel or anti-parallel with the fixed layer magnetization, depending on the direction of current flow.

The behavior of the magnetization of the nano-magnet can be modeled using the Landau–Lifshitz–Gilbert equation with spin-transfer torque term [71]

$$\frac{d\boldsymbol{m}}{dt} = \overbrace{-|\gamma|\,\boldsymbol{m}\times\boldsymbol{H_{eff}}}^{\text{precession}} + \overbrace{\alpha\boldsymbol{m}\times\frac{d\boldsymbol{m}}{dt}}^{\text{damping}} + \underbrace{|\gamma|\left|\frac{\hbar}{\mu_0 e}\right| P\frac{J}{t_m M_S}(\boldsymbol{m}\times\boldsymbol{m_P}\times\boldsymbol{m})}_{\text{spin-transfer torque}} \qquad (3)$$

$\boldsymbol{m}$ is the magnetization vector of nano-magnet, γ is the gyromagnetic ratio, $\boldsymbol{H_{eff}}$ is the effective magnetic field, and α is the damping factor. $\hbar$ is the reduced Planck constant, e is the electron charge, J is current density, t_m free layer length in the direction of current flow, Ms is the saturation magnetization of the magnet, P is the polarization efficiency factor, m_p is the spin polarization of the fixed layer. The first term in (3) describes the magnetization *precession* resulting from effective magnetic field. The second term describes the *damping* that aligns $\boldsymbol{m}$ with $\boldsymbol{H_{eff}}$. Finally, the third term describes the current-induced STT.

B. Domain Wall Strip

Fig. 2 shows a ferromagnetic wire, called domain wall stripe (DWS), with a nanowire-like geometry and opposite magnetization at its two ends. The magnetization transition region along the DWS from one direction to the opposite direction is called domain wall (DW), whose structure and size are dependent on

the DWS geometry and material properties. Typical DW structures in a DWS are also shown in Fig. 2[16], . Magnetic domains lie along the wire axis (in-plane magnetic anistotropy, IMA, domains) in materials where the shape anisotropy dominates (such as Permalloy, NiFe, or Py). The DW can be either transverse or vortex domain wall. The former DW structure occurs in thin and narrow nano-strips whereas the latter occurs when the nano-strip is wider and thicker [16], [17]. The domains are magnetized in the out-of-plane (perpendicular) direction in materials with strong perpendicular magnetic anisotropy (PMA) such as Co/Ni magnetic multilayers. DWs in PMA-based DWS can be either Neel-type narrow DWS or Bloch-type in wider DWS. The direction of DW rotation (or its *chirality*) is energetically degenerate such that left- and right-handed rotations of the DW are equally likely to occur. However, in the presence of broken inversion symmetry, Dzyaloshinskii–Moriya interaction (DMI) [18], [19] can favor and stabilize a particular DW configuration [20]–[22].

Current-induced domain wall motion (CIDWM) due to STT have been observed in DWS [23]–[25]. In the DWS, when the electrons are injected through a fixed domain, they become spin-polarized and exert STT on the DW. This torque induces the rotation of magnetization to the hard-axis direction, resulting in the pinning force. If the current density is above a certain threshold, the STT can overcome this pinning force, leading to steady domain wall motion (DWM). The critical current density-$j_{th} \propto K_{h.a.}\Delta$, where $K_{h.a.}$ is hard-axis anisotropy and Δ is the domain wall width. The hard-axis anisotropy of a PMA device reduces with smaller device thickness and becomes much lower than that of an IMA device. Moreover, the DW width in a PMA device is in general narrower than that in an IMA device. Thus, a scaled PMA magnetic nano-strip has a much lower j_{th} than IMA magnetic nano-strip. Earlier CIDWM experiments on IMA ferromagnetic nanowires showed the critical current density of DWM was in the order of 10^8 A/cm^2 [23]–[25]. This current density causes excessive Joule heating and also causes reliability concerns such as electromigration [23]–[25]. PMA nano-wires on the other hand can have much lower j_{th}[26], [27], which is better for mitigating electromigration issues and for energy consumption. Consequently, most of the recent research has been shifted to PMA nanowires.

III. Neuromorphic Computing Using Spin-Transfer Torque Devices

The "neurons" connecting to each other and to external stimuli through programmable "synapses" are the fundamental computing units of neural network [38]. The basic operation of an artificial neuron involves summing the N weighted inputs and passing the result through a thresholding function. The spin-transfer torque devices discussed in Section II can be used to realize energy efficient analog summation/integration and thresholding operations with the help of appropriate circuits [39]–[42]. Thus, this direct mapping to the operation of biological neuron leads to ultra-low power neuromorphic computation hardware by exploiting the spin-based neuron.

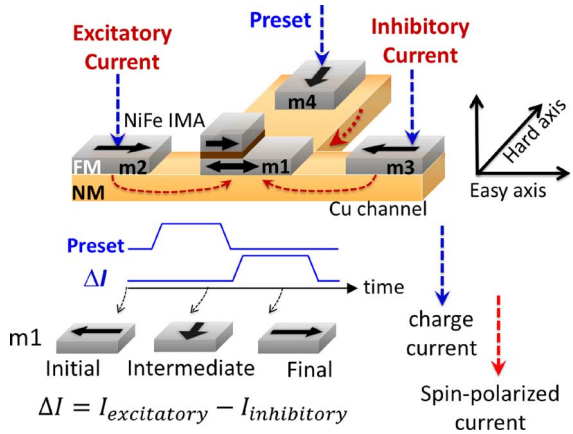

Fig. 3. Spin neuron based on LSV with two complementary inputs and its output magnet (m1) sate.

A. Spin-Neuron Based On Lateral Spin Valve

The device structure of bipolar spin-neuron based on lateral spin value (LSV) is shown Fig. 3, where all of the ferromagnetic contacts (*m1-m4*) are deposited on top a nonmagnetic (NM) channel [13]–[15], [39]. The input magnets (*m2-m4*) are acting as spin injectors and the output magnet (*m1*) forms a MTJ-based read port with a fixed magnet. The spin polarity of magnet *m2* and *m3* are anti-parallel and lie along their easy axis, while the preset magnet—*m4* has its easy axis orthogonal to that of *m1*. The input magnet *m2* (or *m3*) takes the excitatory (or inhibitory) synapse current, while the preset magnet—*m4* is used for implementing current mode Bennett clocking [39]. The operations of this bipolar spin-neuron can be divided into two steps—*preset* and *thresholding*. For the initial preset step, a charge current pulse through *m4* gets spin-polarized and presets the spin-polarity of *m1* along its hard-axis. After removal of the preset pulse, the input magnet *m2* and *m3* take the excitatory and inhibitory synapse currents, which make *m1* switch back to its easy axis because of the STT from the spin-polarized currents. In the end, the final spin polarity of *m1* depends upon the difference ΔI between the excitatory synapse current and inhibitory synapse current. Hard axis, being an unstable state for *m1*, even a small value of ΔI, effects deterministic easy-axis restoration. The MTJ-based read port has a larger effective resistance when the spin polarity of *m1* is anti-parallel to the fixed magnet and vice versa, which can be sensed by a dynamic CMOS latch. Therefore, the spin-neuron based on LSV can efficiently implement the thresholding operation of the total synapse currents.

B. Domain Wall Strip As Synapse

In neural network, the neurons are connected to each other through programmable synapses that are used for weighting operation of the input stimulus. In order to cooperate with the spin-neuron described in previous subsection, the authors in [39] also proposed the use of domain wall strip as synapse, where its programmable spin injection strength is used for implementing spin mode weighting operation. Fig. 4(c) shows a DWS interfaced with the nonmagnetic channel of a neuron MTJ.

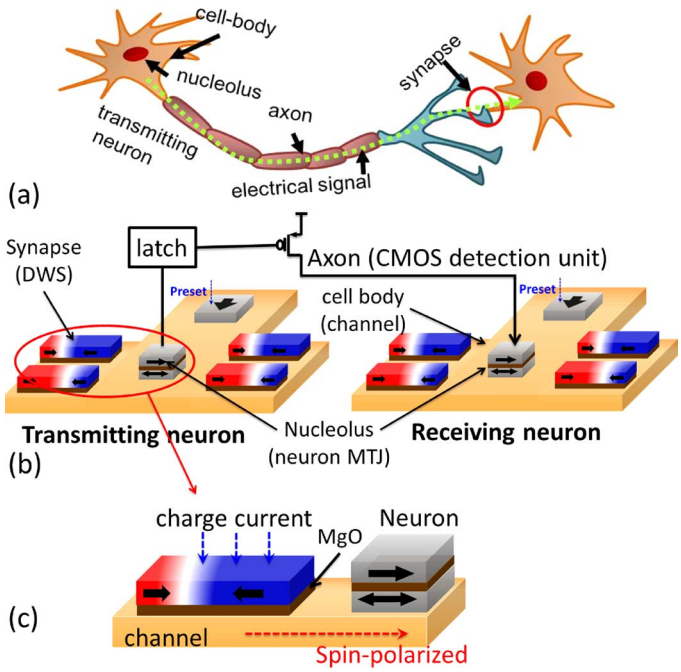

Fig. 4. (a) Biological neural network, (b) one to one mapping of biological neural network using spin-CMOS hybrid neural network, (c) domain wall strip as synapse, where its programmable vertical current spin injection strength is used for implementing spin model weighting operation.

During computation, the input charge (synapse) current is injected into the channel through the DWS in the vertical direction. The spin polarization strength and direction of the vertical charge current reaching the channel is proportional to the offset of the domain wall location from the center [39]. For the extreme left location of the domain wall, the charge current reaching the metal channel is maximally left polarized and vice-versa. The net spin polarization is reduced to zero for the central location of the domain wall, as equal amount of left and right spin electrons are injected into the channel in this case. The output neuron MTJ free layer magnetization is determined by the net STT coming from all of the synapses as described in the operation of spin-neuron based on LSV. Thus, the position of domain wall along the DWS is encoded as the weight of the synapse. The domain wall position (weight) is programmed by the current injection along the length of the DWS, during which the channel is kept in a floating state. Hence, writing and computation modes are fully decoupled. The incorporation of notches along the length of the DWS synapse can help in achieving larger number of weight levels with higher writing accuracy. Note that, a thin MgO layer is incorporated between the DWS and the channel to enhance spin injection efficiency by reducing the spin resistance mismatch between the channel and the magnet [47]. On the other hand, it also reduces the fringe current passing through the parallel path provided by the floating channel during the write operation.

Fig. 4(a) and (b) depicts the one to one similarity between the biological neural network and the spin-CMOS hybrid artificial neural network (ANN) based on the DWS synapse and LSV spin-neuron. The spin potential of the metal channel, analogous

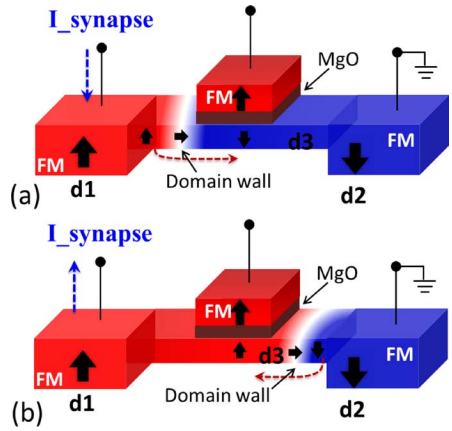

Fig. 5. Device structure of DWN when d3 is parallel or anti-parallel to d1, corresponding to different synapse current directions.

to neuron cell body, can be related to the electrochemical potential in biological neuron's cell body [48]. The dynamic CMOS latch is used to sense the state of current neuron MTJ and drives a distributed set of current source transistors providing supply current to all receiving neurons through the respective DWS synapses. The supply voltages of the source terminal of current source transistors and the ground lead of the spin-neuron modules are $V + \Delta V$ and V volts, respectively. Thus, the synapse current flows across a small terminal voltage of ΔV (~ 30 mV), leading to current model and ultra-low power consumption in inter-neuron communication

C. Spin-Neuron Based On Domain Wall Strip

Fig. 5 shows another spin-neuron based on DWS, which is called domain wall neuron (DWN) [40], [41]. A thin and short nano-magnet domain, *d3* (the "free domain") connects two anti-parallel fixed nano-magnet domains, *d1* and *d2*. Unlike the bipolar spin-neuron in Fig. 3, DWN is a unipolar neuron model, where *d1* is the input port and *d2* is grounded. The total synapse currents are injected through *d1*. As described in Section II, the spin polarity of the free domain (*d3*) can be written parallel or anti-parallel to *d2* depending on the direction of current injected from *d1* (Fig. 5). The state of *d3* can be read through the MTJ formed between a fixed polarity magnet and *d3*. The effective resistance of the MTJ is smaller when the MTJ fixed magnet and *d3* have the same spin polarity and vice-versa, which can be detected by a dynamic CMOS latch. Thus, the DWN can detect the polarity of the current flow at its input node. However, a small hysteresis in the DWN switching characteristics arises from the nonzero current threshold for DW motion. In order to make it closer to an ideal step function, the critical current of domain wall motion can be reduced by device scaling and lowering the magnetic anisotropy barrier.

D. Memristor Crossbar Array As Synapse

In the ANN model, the inputs go through the associated synapses (multiplied by weights) and are summed up as input to neuron transfer function. This operation can be implemented efficiently using a memristor crossbar array (MCA) combined with the previous described domain wall neuron. Fig. 6 shows

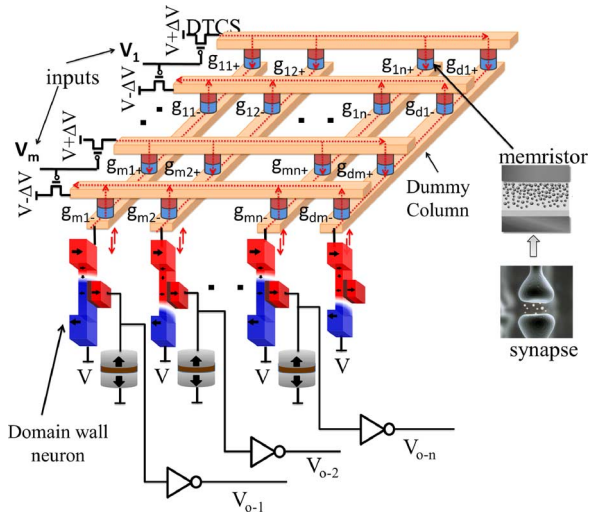

Fig. 6. One layer feed-forward spin-CMOS hybrid neural network using MCA-synapse and domain wall neuron.

the one layer of feed-forward artificial neural network using MCA as synapses and DWN as neurons [40], [41], [46]. In MCA, the conductance (g_{ij}) of a memristor, interconnecting two sets of metal bars, is programmed to the corresponding synaptic weight. One terminal of the DWN is connected with the input synapses, while the other terminal is connected to a fixed voltage V. Due to low resistance of the magneto metallic write path of the DWN, in absence of any input signal, the input terminal of the neuron is also clamped to the same voltage potential.

In the biological neural network, the electrical-chemical signals are transmitted between neurons through "axons" [38]. In Fig. 6, the interconnection between the domain wall neurons are implemented by deep triode current source (DTCS) PMOS transistors. In order to make sure the transistors work in the deep-triode region, the drain to source voltage of DTCS is of the order of few tens of millivolts. The drain to source current, I_{ds}, is fairly linear proportional to Vdd-V_T-V_g, where V_T is the threshold voltage and V_g is the gate voltage. Therefore, DTCS transistor can transmit the neuron output voltage (V_g) into synapse current (I_{ds}) similar to "axon." Fig. 6 shows the spin-CMOS hybrid feed-forward ANN (one layer) hardware design using DTCS-axon, MCA-synapses and domain wall neuron, which shows one to one similarity to biological neural network. In this system, the ith voltage input (V_i) to the MCA synapses connect to the jth domain wall neuron with either positive (g_{ij+}), negative (g_{ij-}) or zero weight. For zero weight (i.e., no connectivity), both g_{ij+} and g_{ij-} are programmed to high resistance "*off*" state. As shown in Fig. 6, the source terminal of DTCS-axon is connected to a voltage potential of $V + \Delta V$ (for positive weights) or $V - \Delta V$ (for negative weights), where ΔV can be $\sim 50mV$. Ignoring the parasitic resistance of the metal crossbar (for small scale network size), the current goes through one synapse can thus be written as $I_{in}(i) \cdot g_{ij}/g_{\mathrm{TR}}$, where $I_{in}(i)$ is the current supplied by the ith DTCS transistor, g_{ij} is the synapse weight dependent conductance of the ith input to the jth neuron and g_{TR} is the total conductance (of all the memristors) connected to a horizontal bar (dummy memristors are added such that g_{TR} is equal for all horizontal bars). Therefore, the current coming out of each MCA in-plane bar is the total current going into the corresponding domain wall neuron, which can be expressed as $\Sigma I_{in}(i) \cdot (g_{ij+} - g_{ij-})/g_{TR,}$. This current determines the domain wall neuron state, which is detected using a high resistance voltage divider formed between a reference MTJ and the DWN read MTJ.

The previous described spin-neurons can also be employed in the design of other different classes of neuromorphic architectures, where large number of neurons can be connected in various network topologies, such as cellular neural network [44], convolution neural networks [45], and hierarchical temporal memory [42].

IV. Computing Using Coupled Spin Torque Nano-Oscillators

In this section, we present the basic device structures of STNOs [49]–[52] and the coupling phenomenon between multiple STNOs [58]–[65]. Such coupled STNO array can be used in non-Boolean computations for image processing applications.

A. Spin-Torque Nano-Oscillator

A standard two-terminal STNO has two ferromagnetic layers separated by either a thin nonmagnetic metal [giant magnetoresistance (GMR)] or a thin insulating oxide (TMR). One of the ferromagnetic layers has a fixed magnetization, while the other one is called "free layer" in which the magnetization can be influenced by a charge current passing through the device and/or by an applied magnetic field. This device offers lower resistance when the spin polarity of the free layer is parallel to the fixed layer compared to that of the anti-parallel state. When the charge current is injected into the device, the electrons become spin-polarized because of the high polarity fixed magnetic layer. The spin-polarized electrons exert STT in the free layer, as described in Section II. The dynamics of the free layer is governed by Landau–Lifshitz–Gilbert (LLG) equation with a Slonczewski's torque term (1). For a given static magnetic field, the free layer spin polarity can be set into steady state precession, biased with a constant charge current. Under such a condition, the STT due to the charge current and the inherent damping torque balance out each other, preventing the bi-stable switching transition. The resistance of spin valve can be expressed as a function of relative angle (θ) between the spin polarizations of the two ferromagnetic layers, as shown in (2).

Recently, several other three-terminal STNO structures, such as spin hall effect (SHE) STNO [66]–[70] and dual pillar (DP) STNO [58], have been proposed. In SHE-STNO, a MTJ is milled on the spin hall metal nano-strip. When a charge current is applied along the spin hall metal nano-strip, it injects spin current into the MTJ free layer, leading to a sustained oscillation. The output voltage oscillation can be obtained by passing a read current through the MTJ. The device structure of SHE-STNO offers separate control of frequency and output oscillation amplitude. Thus, the output voltage swing can be tuned without disturbing the frequency. Another three-terminal STNO, DP-STNO, also comes with decoupled bias and read

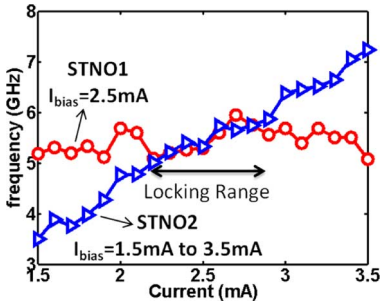

Fig. 7. Frequency versus current plot for two spin wave coupled STNOs, showing the locking range.

paths [58], where an extended free layer is shared by the low resistance, magneto-metallic GMR interface and a high-resistance TMR interface. The GMR interface is used for biasing that allows the application of low bias voltage. The TMR interface is used for sensing to obtain a large output voltage swing.

B. Frequency/Phase Locking Mechanisms of Multiple Stnos

The frequency/phase locking of multiple STNOs can be obtained through magnetic coupling [58]–[61], electrical coupling [62], or injection locking mechanisms [63]–[65]. Magnetic coupling may involve the spin wave interaction through a shared magnetic substrate [12] or dipolar fields exchange of physically isolated STNOs lying in close proximity. Thus, only small number of STNOs can be synchronized through magnetic coupling because of geometrical constraints. Fig. 7 shows the frequency locking property of two STNOs coupled through spin wave interaction. The DC bias of STNO1 is kept constant, while the dc bias of STNO2 is varied. The frequency of STNO1 is almost constant (variation because of thermal noise), whereas, the frequency of the second STNO increases with its dc bias current. The two STNOs oscillate independently, when the frequencies are far apart. They acquire phase and frequency lock when their frequencies lie in *locking range*, as depicted in Fig. 7. In a STNO array, if each output oscillation signal is combined into a broadcast signal and superposed to the dc driving current of each STNO, the frequency locking of this STNO array can be obtained by this electrical connectivity [62]. The other locking mechanism is called injection locking [63]–[65], where multiple STNOs get frequency/phase lock through the injection of an external microwave signal (ac current or field) close to the STNO free running frequency. Compared with magnetic coupling, electrical coupling and injection locking mechanism can be employed for synchronization of large numbers of STNOs.

The coupling phenomenon of multiple STNOs is attractive for ultra-low power non-Boolean computation for image processing applications [53]–[58]. Fig. 8 shows a 3×3 STNO array with spin wave based nearest neighbor coupling, which can be employed for image edge extraction [58]. All of the STNOs in the array were in a locked state by a common biasing current and spin wave coupling at the initial computing state. Then, the dc bias current of each STNO is shifted a value that is proportional to the pixel intensity of the corresponding 3×3 image window. If the input image window is in the edge region, the current inputs of the STNO array are different enough

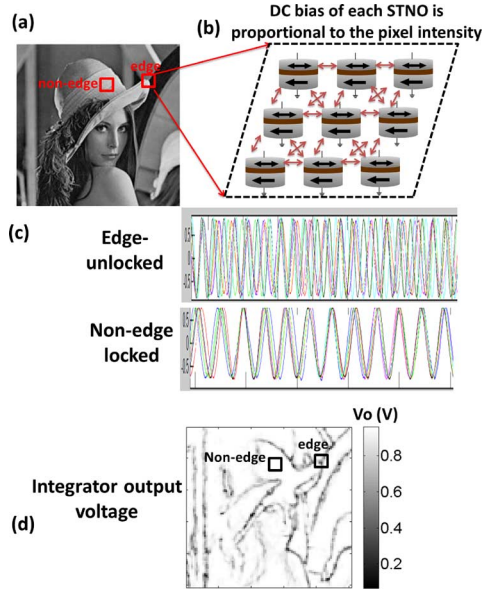

Fig. 8. (a) Input grey-scale image, (b) Schematic of 3×3 STNO array with magnetic coupling between nearest neighbors, (c) the transient output waveforms of STNO array for unlocked and locked cases, (d) the integrator output voltages of coupled STNOs array indicating the edge plot of the input image.

to induce large frequency shifts of STNOs, leading to upset the locking. Fig. 8(c) shows the nine STNO transient output oscillations for unlocked and locked state, corresponding to the "edge" and "nonedge" image regions. The outputs of the STNO array are capacitively added and applied to a CMOS integrator design. The summation of locked STNO array leads to a regular waveform and faster charging of integrator, while the unlocked STNO array induces an irregular waveform and slower charging of integrator. Thus, given a constant charging time, the high integrator output voltage indicates the nonedge region of the image (locking of the STNO array), as shown in Fig. 8(d). Another promising application is the associative pattern matching, where the degree of match (DOM) between two analog vectors is evaluated by exploiting the input dependent locking characteristics of the coupled STNOs array [53]–[57].

V. Reconfigurable In-Memory Computing

Memory arrays built with STT devices are highly promising for building energy-efficient reconfigurable computing platforms. A number of nonvolatile reconfigurable frameworks employing STTRAM as the primary storage element have been proposed earlier [85]–[87]. All these architectures employ a spatial computing model similar to conventional FPGAs, where the STTRAM is used to store the configuration in small 1-D lookup tables (LUTs). This has two major limitations: 1) it fails to exploit the high integration density of the STTRAM array; 2) the requirement for CMOS-STTRAM hybridization at the location of each configuration bit poses serious challenge in fabricating the proposed architectures. These limitations can be effectively addressed while leveraging the integration and access performance/energy benefits of large STTRAM array in an alternative memory-based reconfigurable hardware platform. We call it memory-based computing (MBC) platform that favors mapping multiple-input multiple-output functions

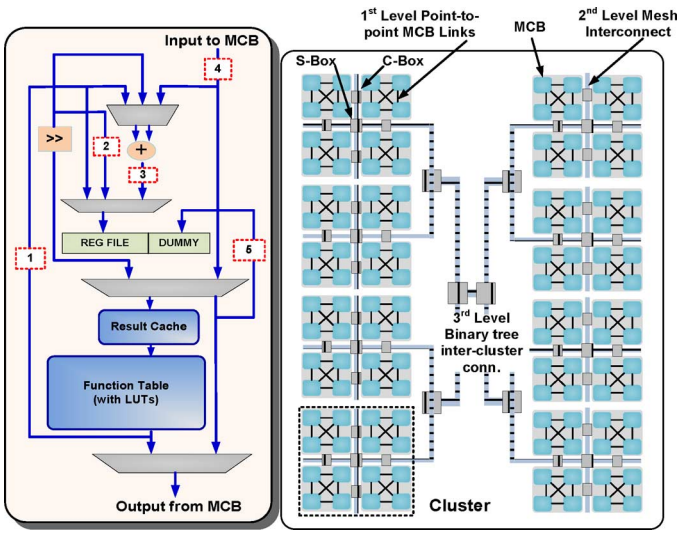

Fig. 9. MCB micro-architecture (left) and a MBC platform with multiple hierarchically-connected MCB units (right).

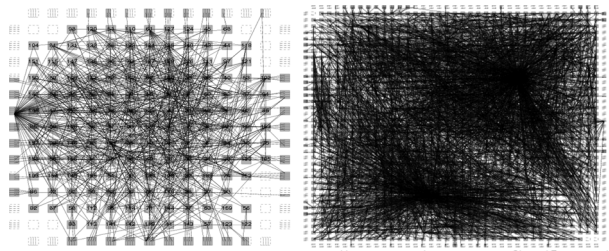

Fig. 10. Comparison of programmable interconnect requirement: (left) MBC, (right) FPGA.

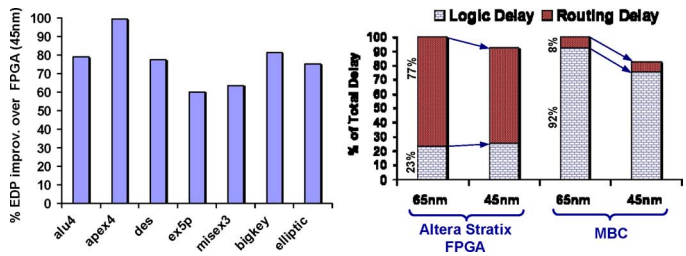

Fig. 11. EDP improvement in MBC over FPGA at the same technology (45 nm) for fine-grained applications (left). Technology scalability of performance for FPGA and MBC.

as LUTs in a large 2-D memory and then evaluating them in a spatio-temporal manner [73]–[77].

A. Nonvolatile MBC Using Sttram

The primary concept behind MBC system is to use a dense 2-D memory array to map logic functions and evaluate them in time-multiplexed and topological fashion using a small controller designed using regular logic structure. The controller can be realized with either CMOS or STT device based logic circuits. It departs from both standard logic based or FPGA-based information processing system as MBC uses a large and dense embedded memory array for processing (not logic gates or small LUTs).

Fig. 9 illustrates the architecture of a memory based computing system. The computational building block (shown left) in the MBC platform referred as memory-based computational Block or MCB (similar to CLB in FPGA) consists of the following three major components: *the schedule table* (a small memory that holds the partitions), *the function table* (a large memory array that holds the LUTs), and the *controller module*. MBC minimizes overhead from programmable interconnects (PIs) due to two reasons: 1) partitioning the target application into large multi-input multi-output partitions which are mapped to the memory array inside each MCB; and 2) local multi-cycle execution inside each computing element. An example of reduction in PI is shown in Fig. 10 for an ISCAS-89 benchmark circuit s38417. MBC is expected to provide the following major advantages over conventional FPGA-based spatial computing framework: 1) higher integration density, 2) higher energy efficiency, 3) better reliability under high defect or parameter variability induced failures as well as transient failures such as soft errors, and 4) higher scalability of performance across technology generation. The last point is illustrated in Fig. 11, which shows the energy delay product (EDP) improvement with MBC compared to FPGA and compares performance scaling across two technology generations between FPGA and MBC. Due to reduced impact of PIs in performance, MBC can achieve considerably better performance scaling than a PI-dominated FPGA architecture.

In the nonvolatile MBC framework, we can build the function table and schedule tables using STTRAM arrays. This offers the following benefits: 1) since the function table holds the configuration for the partitions, it occupies the maximum area inside a MCB. However a small footprint for the MTJ devices [84] ensures that the area occupied by this memory array is minimized; 2) nonvolatile nature of the STTRAM array ensures that configuration bits for the logic (stored in the function table) and for the local interconnects (stored in the schedule table) is retained when power is turned down; 3) high read performance and low read power for the STTRAM array results in considerable EDP improvement for a STTRAM-based nonvolatile MBC framework.

B. Circuit/Architecture Co-Optimization Techniques

The design space for STTRAM is constrained by the readability and writability conditions i.e., TMR ratio and write current requirement. Given a MTJ, the choice of the access MOSFET width (W) and its wordline voltage (V_{WL}) can be used to navigate the design space of TMR and write-current. To minimize the energy dissipation, we propose to choose the energy optimal point in the $W - V_{\mathrm{WL}}$ plane. The total energy is evaluated considering the write/read current through the MTJ-transistor structure and the switching energy associated with the wordline and biltine [76]. A key aspect of the solution is its dependence on the read-write probability. Fig. 12(a) shows two solutions corresponding to write probabilities of 0.5 and 0.1, respectively [76]. These two solutions are different because different write probabilities result in different read and write

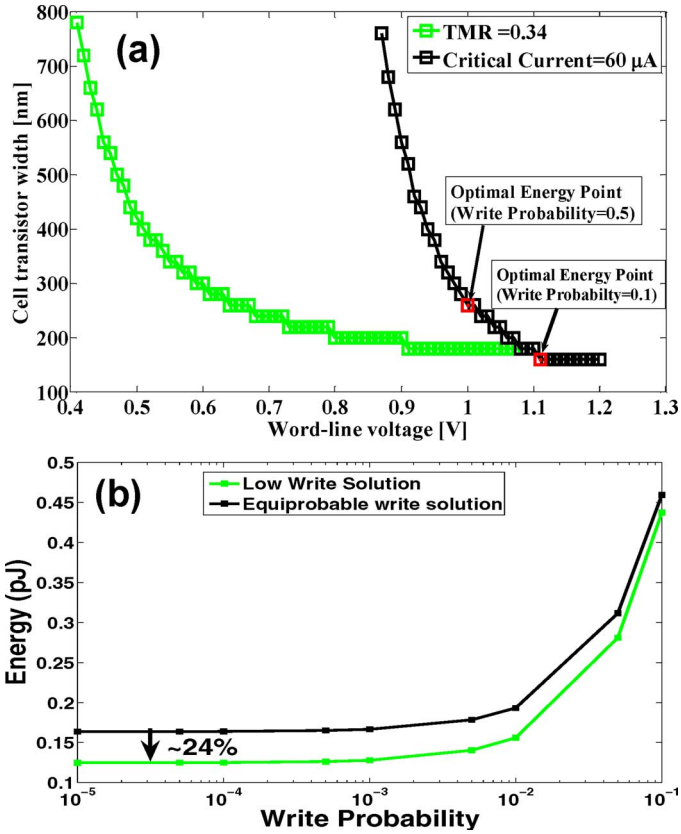

Fig. 12. (a) Design of STTRAM cell for MBC framework; (b) read energy with varying write probability [76].

energies. This reflects a change in the optimization parameters. A larger write probability means a solution with larger width and smaller V_{WL} as write has a quadratic dependence on V_{WL}. From read perspective a solution with lower width is preferred due to less leakage power dissipation. For MBC with read-dominant access pattern, the $W - V_{\mathrm{WL}}$ configuration corresponding to equi-probable condition is not an optimal choice as it dissipates higher read energy [Fig. 12(b)] [76]. Hence we chose the optimal energy point corresponding to low write probabilities which provides much lower read and total energy at the expense of increased write energy [Fig. 13(a) and (b)] [76]. Fig. 12(b) shows 24% saving in total energy for write probability of 10^{-5} for an 8-bit 64×64 memory array with a read access time of 400 ps [76].

From the STTRAM read operation we find that a larger current flows in the circuit corresponding to read '0' than read '1'. This is because resistance of state '0' is lower than state '1'. Thus in Fig. 13(a) there is a 36% difference between energy dissipated in the read '1' and read '0' operations. Write energy for '0' case dominates over the '1' case [76]. However for the MBC application intended, the system is heavily biased towards read with a write probability in the range of $10^{-3} - 10^{-5}$. Hence for MBC application, we conclude that if the system is biased for more read '1's than '0's we can have considerable energy savings with STTRAMs [76].

Due to higher read power during a read '0' operation, it is intended that the STTRAM array contain more logic '1' than logic '0'. Considering this asymmetry, we have developed a "preferential mapping" approach to skew the LUTs to contain more logic '1' than logic '0' in order to harness the energy advantage as seen in Fig. 13(a). Such a preferential application mapping scheme therefore amplifies the energy savings by storing more logic '1' than logic '0' in the schedule and function tables. The greedy heuristic for skewing the logic '0' to logic '1' ratio in the LUTs as presented in [87] is used to exploit the lower read '1' power in the STTRAM-based MBC framework. The effectiveness of the preferential mapping approach was validated for a set of standard benchmark circuits chosen from MCNC benchmark suite. For the selected benchmark circuits, the preferential mapping heuristic was observed to achieve on an average about 49% increase in the logic '1' count stored in the LUTs.

From these discussions we conclude that as the number of '1's stored in the array increases the energy advantage will keep on increasing. A study on STTRAM array energy with varying probability of '1' storage is shown in Fig. 13(c) [76]. It points to the fact that a solution with all zero storage will result in a 16% energy access overhead compared to the case when all ones are stored in the array.

C. Simulation Results

We have performed simulations with MTJ at 65 nm node with resistance-area product 30 Ω-$\mu\mathrm{m}^2$[76], [77]. The sizes of the MTJ devices have been taken as $50 \times 90\ \mathrm{nm}^2$ which requires approximately $60\mu A$ of switching current assuming current density of $10^6\ \mathrm{A/cm}^2$. The high and low resistance states are represented by 11.1 kΩ and 6.67 kΩ, respectively. The transistor was designed so as to be able to drive the switching current under both write '0' and write '1' conditions.

To obtain the solution for varying write probabilities, first a host of simulations with the high and low resistance is performed for a range of V_{WL} and W. The solution space has to be extracted from the generated design space considering the constraints on minimum TMR and switching current. In this work we consider minimum TMR and switching current requirements of 0.34 and $60\mu A$, respectively. Corresponding to this extracted feasible design space of $V_{\mathrm{WL}} - W$, we evaluate the read, write, active leakage and total energy of STTRAM array. The energy evaluation considers the read and write probability ratios. The $V_{\mathrm{WL}} - W$ combination which gives the minimum energy is identified as the optimal energy solution. For demonstration of the results we selected write probabilities of 0.5 and 0.1 to evaluate the design points. The read and write energies for '0' and '1' are computed for these design points.

Delay and energy requirement for the CMOS elements of the MCB were obtained through SPICE simulations using BSIM4 predictive models at 65 nm technology [82]. A supply voltage of 1 V was used for simulation. As the cycle time for a given benchmark in the MBC framework depends on the delay through the programmable interconnects, interconnect delay for both MBC and FPGA frameworks were obtained from the VPR toolset [83]. A 65 nm FPGA model [88] was used to simulate the performance of the programmable interconnects.

Fig. 14(a) and (b) shows the improvement in performance and energy-delay product for STTRAM-based MBC over CMOS FPGA framework [76]. As we note from Fig. 14(a), for standard benchmark circuits on an average the MBC framework

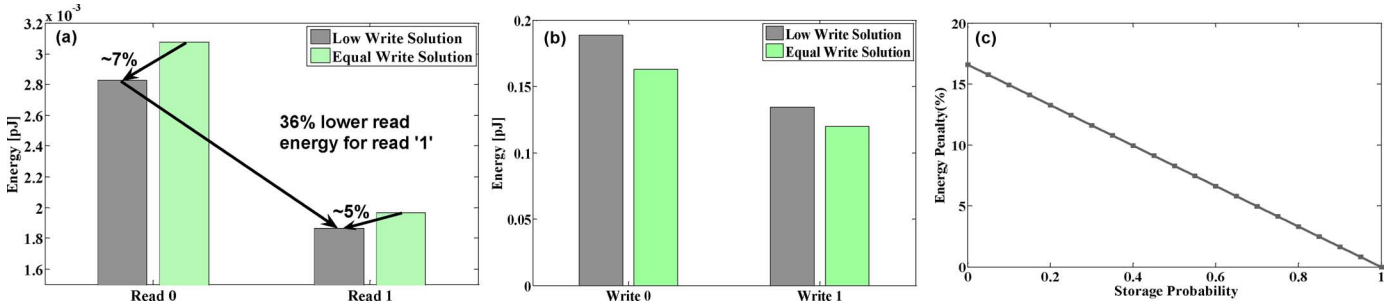

Fig. 13. (a) Read and (b) write energy for a cell storing logic '0' and '1'. (c) Increase in read energy with increasing probability of storing '1' [76].

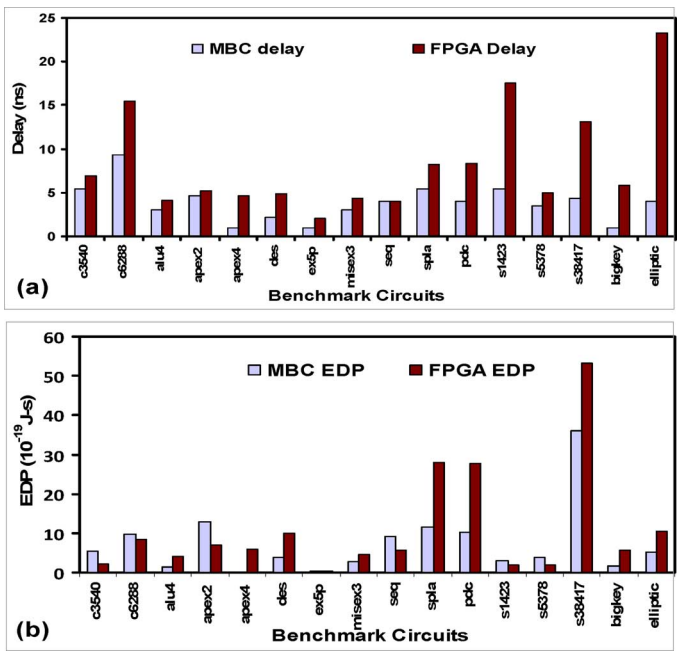

Fig. 14. Improvement in (a) delay and (b) EDP for STTRAM MBC over conventional SRAM-based FPGA [76].

improves the performance by 45.4%. Fig. 14(b) compares the EDP values between the two frameworks. The nonvolatile MBC framework achieves a 5% improvement in EDP over the CMOS FPGA framework. The performance and EDP computation includes the cell optimization for read operation. The EDP improvement is further enhanced through the preferential mapping step which skews the LUT contents to have more logic '1' than logic '0's. As a result of this preferential mapping, the average EDP improvement was calculated to increase from 5% to 6.64%.

STTRAM holds tremendous promise as a nonvolatile memory for storing the configuration bits in a reconfigurable computing framework. MBC frameworks which use dense 2-D STTRAM array as a configuration memory are nonvolatile and have higher energy-efficiency compared to STTRAM-based FPGA frameworks. Moreover, high read performance and low read power for the STTRAM arrays translate into considerable improvement in EDP for STTRAM-based MBC over conventional CMOS-based FPGA framework. This improvement can be further enhanced by circuit/architecture co-optimization techniques, which involve preferential design of the MTJ cell and skewed application mapping step that increases the number of logic '1's over logic '0's in the LUT content.

VI. Conclusion

We have explored several energy efficient unconventional computing models (neuromorphic computing, non-Boolean computing and in-memory computing) using ultra-low voltage, current mode operation of spin-transfer torque devices. Such devices may be integrated with CMOS and other charge-based devices to develop highly energy efficient computing systems in the beyond-CMOS regime. The spin-transfer torque devices are unlikely to be drop-in replacements for CMOS. Hence, there is a need for rethinking the circuit, architecture and computing models that are inherently suited to the characteristics of the devices, and new applications that are enabled by their unique capabilities to truly leverage spin-transfer torque device based computing. Device-aware circuit and architecture level design approaches, which takes advantages of the unique features provided by spintronic devices can be attractive in minimizing energy and improving performance as well as reliability of next-generation computing systems.

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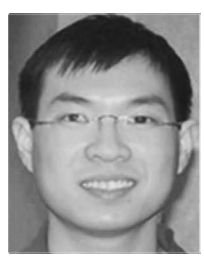

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