Nanomechanical Non-Volatile Memory for Computing at Extreme

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***Abstract*— A computing platform that works under extreme conditions ($> 250\,^{\circ}\mathrm{C}$ and at radiation > 1 Mrad) can be attractive in a number of important application areas, including automotive, space and avionics. Nanoelectromechanical systems (NEMS) switches have emerged as promising candidates for computing in harsh environment. Designing reliable memory specifically non-volatile memory is a major challenge for these computing systems. In this paper, we propose a novel non-volatile memory (NVM) design for reliable operation in extreme environment using NEMS structure. It exploits a common failure mode in these devices, namely stiction. Unlike traditional charge-based memories, it relies on the mechanical state of a NEMS switch as information carrier. We analyze device and circuit-level design issues to enable robust NVM array implementation with NEMS devices.**

I. Introduction

Computing platforms capable of operating at extreme environment - specifically at temperatures $> 250\,^{\circ}\mathrm{C}$ and high radiation (1-30 Mrad)- are attractive in several applications, including advanced propulsion systems, high-temperature (HT) measurement and control instrumentation. Existing wide-band-gap semiconductors, e.g. silicon carbide junction field effect transistor (SiC-JFET) electronics have been considered most viable for HT applications. However, the large size, low switching speed, and high leakage current make these devices unattractive for these applications. Also, the leakage current markedly increases with temperature. This has motivated investigations on alternative NEMS logic circuits for extreme environments [4].

Memory sub-circuits are an integral part of modern computing and storage platforms. Building memory circuit for extreme conditions is more challenging than logic. This is because conventional charge-based memory (both volatile such as DRAM, and non-volatile such as NAND-flash) fails to retain data under such conditions. Furthermore, negative threshold SiC-JFET devices are typically not suitable for robust memory design. A non-volatile memory (NVM) technology that can work robustly at extreme conditions with virtually zero leakage power can address this critical need.

In this paper, we propose a novel NVM array for extreme conditions using NEMS switches. Unlike the conventional charge-based memory, it stores logic values based on the mechanical state of a cantilever beam. It exploits a common failure mechanisms in NEMS switches, namely *stiction*, that creates an irreversible contact between the beam and gate/drain electrodes. Fig. 1a) and b) show the 3D cell structure and scanning electron microsope (SEM) image of the proposed device obtained from a fabrication run. Using a 5-terminal (5T) switch configuration that allows active pull-off of the beam, we can realize one-bit storage with just one active element (i.e. the beam), which is used as a bi-stable memory cell (Fig. 1c and Fig. 1d). The read-out operation senses the position of the beam by passing a current between source and drain terminals of the switch. Writing is accomplished through electrostatic actuation of the beam by controlling bias voltages in G1 and G2. Using a well-known HT compatible material, namely, poly-silicon carbide (poly SiC) to implement the NEMS switches, the proposed memory can work reliably under high temperature and radiation.

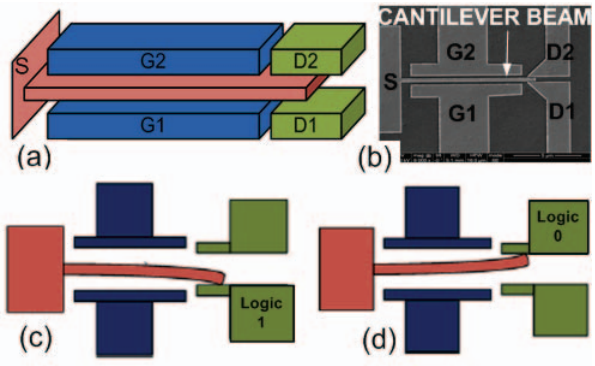

Fig. 1. (a) Schematic of the proposed 5T nanomechanical memory cell; b) an SEM image of the 5T device; c) and d) bi-stable nature of the cells representing stored content of '1' and '0', respectively.

Micro/nanoelectromechanical (M/NEMS) switches have been used to implement memory blocks. Researchers have explored MEMS 3-terminal (3T) switch along with a capacitor [1] to form a memory unit. This NV MEMS cell is similar to a DRAM cell with the MEMS switch replacing the MOSFET select device. Such a capacitance based device adds large area overhead to a cell and is prone to charge leakage and hence, the value tends to degrade over time leading to increased soft error vulnerability and low retention time. Another structure proposed to overcome the capacitor dependence is a NEMS memory that comprises of an Aluminium cantilever beam actuated by an external electrostatic force [2]. The device, however, works on the principle of storing charge in a dielectric stack and thus induces a charge-based shift of the read and write voltages. It inherits similar issues as observed in devices of [1]. To the best of our

978-1-4799-0874-5/13/$31.00

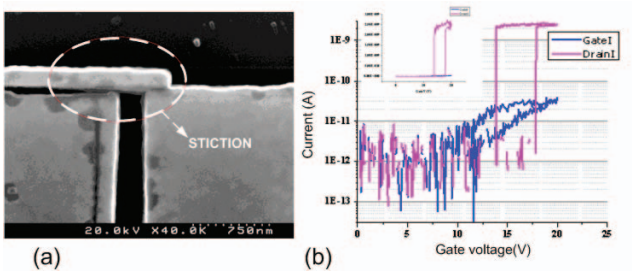

Fig. 2. (a) SEM image showing stiction in a SiC cantilever beam; b) the log plot shows switching characteristics of a typical SiC 3-terminal device with 8μm length beam and 250nm gate-source gap (inset: linear plot).

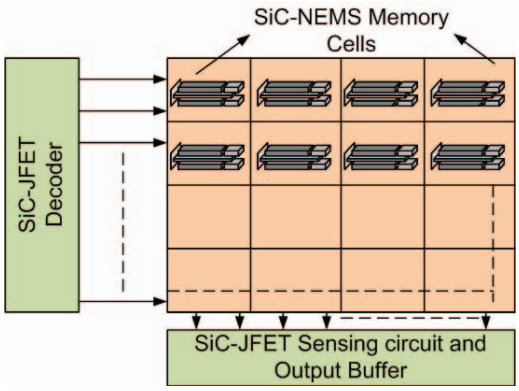

Fig. 3. Block diagram showing JFET-NEMS integration to realize memory array: JFET peripheral electronics and NEMS 5T memory cells.

knowledge, none of the existing works on nanomechanical memory target operation at extreme conditions. Most charge-based memory units do not lend themselves for use in these conditions primarily due to leakage issue. Although wide-band-gap semiconductors can be used to design memory for operation at these conditions, they are volatile and hence is not suitable for long-term data storage.

II. Memory for Extreme Environment

A. Choice of material and structure

We use SiC NEMS cantilever based switch structure to realize non-volatile memory cells that stores information using mechanical state of the switch. SiC is a semiconductor material known to be highly suitable at extreme conditions due to its excellent thermal stability and chemical inertness. We use a 5T switch structure with two gates, which act as the pull-in and active pull-off terminal, respectively.

B. Operating principle

We exploit *stiction* (Fig. 2a) a commonly observed failure mechanism in NEMS to store values by maintaining contact between beam and drain electrode. The main forces acting on a cantilever beam are electrostatic force (Ee), which arises due to gate actuation voltage (V_{pi}), mechanical restoration force (Em), and the van der Waal's force between two surfaces in contact [4]. To write logic '1', V_{pi} is applied at G1. When $Ee > Em$, the cantilever beam bends to touch the drain surface. V_{pi} can be determined using the spring-mass model on the cantilever beam, where $V_{pi} = \sqrt{(8kg^3/27\epsilon_0 A)}$, k=spring constant, ϵ_0=material permittivity, g=G-S gap, A=actuation area. Fig. 2b shows the switching behavior obtained from DC measurement of a fabricated 3T NEMS switch. The switch snapped in at $\sim$18V. On further scaling of these devices V_{pi} as low as 3V can be achieved. Based on device material and structure, we can determine the dimensions and voltage to deterministically cause stiction [5]. To write logic '0' (contact with D2), we apply high pull-off voltage at G2. The device reads value sensing the current at D1. A high current corresponds to logic '1', while near zero current to logic '0'.

C. Hybridization with JFET peripheral circuit

SiC JFET devices are considered attractive for building HT [6] electronics. For the proposed NVM array, we can implement the peripheral logic using SiC JFET devices. Fig. 3 shows the circuit-level hybridization of NEMS memory with JFET peripheral electronics to realize large two-dimensional memory array. This integration incorporates the high gain and driving capacity of JFET along with the complementary low-leakage, robust operation of NEMS devices under high temperature and radiation.

III. Conclusion

We have presented a NEMS NVM array design capable of operating at extreme conditions in terms of temperature and radiation. We leverage on a common failure mechanism in NEMS switches, namely stiction, to realize NVM cells with nanoscale dimensions. Choice of data storage based on mechanical state of a switch along with SiC as material, enables stable memory operation at harsh conditions. Since each nanoscale switch can realize a single level cell, it can provide high density, high endurance, and acceptable read/write speed. Recent research shows over 10^9 switching cycles for a 3T switch [4]. Furthermore, use of just one active element per cell is expected to provide high manufacturing yield. Future work will involve detailed theoretical analysis as well as test of fabricated devices.

IV. Acknowledgement

This work is supported in part by National Science Foundation (NSF) grant # CCF-1116102.

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