High-Temperature (>500°C) Reconfigurable Computing Using Silicon Carbide NEMS Switches

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***Abstract*—Many industrial systems, sensors and advanced propulsion systems demand electronics capable of functioning at high ambient temperature in the range of 500-600°C. Conventional Si-based electronics fail to work reliably at such high temperature ranges. In this paper we propose, for the first time, a high-temperature reconfigurable computing platform capable of operating at temperature of 500°C or higher. Such a platform is also amenable for reliable operation in high-radiation environment. The hardware reconfigurable platform follows the interleaved architecture of conventional Field Programmable Gate Array (FPGA) and provides the usual benefits of lower design cost and time. However, high-temperature operation is enabled by choice of a special device material, namely silicon carbide (SiC), and a special switch structure, namely Nano-Electro-Mechanical-System (NEMS) switch. While SiC provides excellent mechanical and chemical properties suitable for operation at extreme harsh environment, NEMS switch provides low-voltage operation, ultra-low leakage and radiation hardness. We propose a novel multi-layer NEMS switch structure and efficient design of each building block of FPGA using nanoscale SiC NEMS switches. Using measured switch parameters from a number of SiC NEMS switches we fabricated, we compare the power, performance and area of an all-mechanical FPGA with alternative implementations for several benchmark circuits.**

Keywords- High Temperature Electronics; SiC; NEMS; FPGA

I. INTRODUCTION

Electronics capable of working reliably at temperature beyond 500°C can be extremely useful in diverse applications, ranging from aerospace, automotive, energy production, and industrial systems [1-4]. For example, intelligent propulsion systems, spacecraft for Venus exploration and active combustion control require prolonged operation of the sensors and associated circuitry at temperatures exceeding 500˚C. Conventional Si-based Integrated Circuits (ICs) fail to operate at such high temperatures due to intrinsic physical limitation of the transistors to work reliably at these temperatures [4].

The emergence of wide band gap semiconductors such as silicon carbide (SiC) provides an alternative material to develop circuits, which can function at ambient temperatures of 500˚C or higher [2]. Silicon carbide electronics has been widely accepted as the most viable technology for such high temperature applications due to their excellent mechanical and chemical properties [1-2, 4]. Among different alternative device architectures, SiC junction field effect transistor (JFET) has been successfully used for developing high temperature analog electronics such as differential amplifier, which can operate at 600˚C [1]. However, the large size, high leakage and lack of enhancement-mode devices prohibit the use of SiC JFET for developing digital logic elements for very large scale integrated chips [4]. On the other hand, the use of nano-electro-mechanical system (NEMS) switches has been explored as an alternative to conventional transistor-based circuits [5-8]. In particular, SiC NEMS-based inverters have been fabricated and demonstrated to successfully function at high temperatures for billions of cycles [4]. The advantages of NEMS-based electronics have been emphasized earlier by various researchers, primarily in the context of minimizing leakage [5-7]. However, only recently, the application of NEMS devices has been investigated for high-temperature electronics [4].

Although investigation in [4] envisages a custom ASIC implementation, a reconfigurable framework such as Field Programmable Gate Array (FPGA) provides an excellent choice of hardware architecture for high-temperature applications. Although the area/delay/power of FPGA is typically inferior to those of ASIC, they provide an important platform for low-cost, low-volume production with fast turn-around time [11]. Since most current high-temperature digital systems target specific industrial applications requiring low-volume production, it is desirable to use a reconfigurable platform like FPGA. Besides, because the defect rates for NEMS-based electronics is expected to be high – both post-fabrication and at run-time – FPGA provides a more reliable platform for NEMS devices, since applications can be mapped around defects. The major drawback of conventional FPGA compared to ASIC is the relatively high leakage power primarily due to the presence of large number of configuration cells and programmable interconnects. In this context, the NEMS-based building blocks are highly attractive compared to FET-based implementations since NEMS switches exhibit virtually zero leakage [6]. Hence, SiC NEMS-based FPGAs can be a viable option for high-temperature digital electronics.

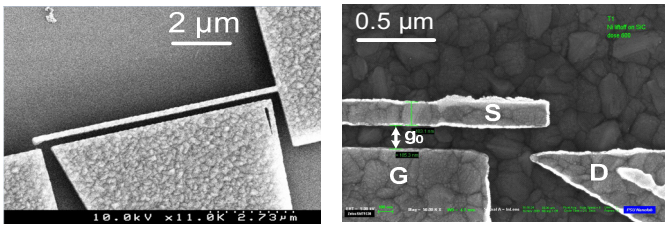

Figure 1. SEM picture of our fabricated laterally-actuated 3-T SiC NEMS switch (left); zoomed version to show the gap (g_0) between the cantilever (S) and gate (G)/drain (D) electrodes (right).

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In this paper, we present a SiC NEMS-based FPGA architecture for high-temperature applications. To the best of our knowledge, this is the first FPGA architecture targeting operation beyond 500˚C. The choice of SiC as material and NEMS switches as device building block provides the enabling technology for high-temperature operation. We propose a novel multi-layer beam NEMS switch structure, which allows efficient implementation (in terms of number of moving elements, performance and power dissipation) of the FPGA building blocks, namely memory cells and multiplexer trees. We explore two alternative FPGA architectures for high temperature operation – one using JFET-based memory elements and NEMS-based interconnects (hybrid JFET-NEMS FPGA) and the other that implements all building blocks using NEMS switches (all-mechanical FPGA). Using the measured parameters from SiC NEMS switches we fabricated, we evaluate the power/performance/area of both architectures and also compare them with conventional CMOS FPGA. We show that an all-mechanical FPGA provides an excellent choice for low-power, reliable operation at high temperature, while maintaining the usual benefits of an FPGA.

II. Background

Due to the increasing demand for electronics for harsh environment high-temperature sensors, there has been widespread research on enhancing Si-based electronics using silicon-on-insulator (SOI) technology (which has been demonstrated to work up to 300˚C [3]) as well as using alternative materials like SiC for building JFET-based analog circuits (which can work up to 600˚C [1]). To avoid the problem of high junction leakage current in Si transistors due to generation of large number of intrinsic carriers at high temperature, people have used SOI technology [3] where the insulator isolates the silicon substrate from the transistor nodes, leading to improvement in off-state current at high temperature and also reducing the possibility of latch-up [1]. However this technology fails to work reliably at temperatures above 300˚C.

Silicon carbide (SiC) is a promising semiconductor for high temperature electronics because of its wide band-gap voltage (~3V), high electric field breakdown and fewer crystal dislocation defects compared to other wide band-gap materials [2]. Among different transistor device structures, junction field effect transistors (JFET) have been most promising in terms of reliable manufacturability and device characteristics as well as large scale integration capability. Poor gate oxide quality due to high oxide-Si interface trap density is a concern for SiC metal-oxide-semiconductor FETs (MOSFETs), while Schottky-based metal-semiconductor FETs (MESFETs) have high gate leakage at high temperatures [2]. Low hole mobility leads to poor performance of p-channel devices and the most mature SiC device in terms of fabrication process and reliable operation at high temperatures is the n–channel depletion mode JFET. However, their large size, high threshold voltage and low switching speed make them unsuitable for logic design, except for stand-alone digital gates. In addition, the high leakage current through off transistors can cause huge power overhead, especially at high temperature.

Using electro-mechanical switches as replacement for the transistors allows the design of static CMOS-like inverters [4], which alleviate the leakage problem because of almost zero off-state current and infinitely steep sub-threshold slope. Since their on-off transitions are governed by electrostatic actuation unlike the carrier depletion of transistor channels, which is highly sensitive to temperature, the NEMS relay-based switches can maintain high off-channel impedance and hence, ultralow leakage even at 600˚C or higher temperatures. Moreover, the switches can be scaled down to nanoscale dimensions for miniaturizing the area and increasing the integration density. The contact resistance of NEMS relays can be made lower than on-resistance of MOS transistors by proper fabrication technique [10]. These NEMS-switches have also been shown to operate at microwave frequencies (up to 1 GHz) for nanoscale device dimensions [14]. A scanning electron microscope (SEM) image of a fabricated SiC 3-terminal cantilever is shown in Fig. 1.

In [5] the authors introduced complementary NEMS switches made of Nickel, based on a tuning-fork structure and proposed several CMOS-like logic gate structures. A 4-terminal NEM-relay was presented in [7], along with a 32-bit full adder design using simpler logic style than static CMOS. In addition, the authors in [8] and [9] provided insights into design considerations of NEM-relay based circuits and NEM-CMOS hybrid circuits, respectively. A carbon nanotube (CNT)-based NEMS memory element for replacing conventional SRAM cells in FPGA LUTs was proposed in [6]. The authors in [10] implemented FPGA routing using NEM-relays for low-power. However, these NEMS-based FPGA designs use NEMS-CMOS hybrid approach or are based on materials which cannot function reliably at high temperatures. Therefore, they cannot be used for high temperature applications. SiC is an extremely suitable material for such applications because of its excellent thermal stability, mechanical robustness and chemical inertness [4]. In this paper, we describe the architecture and switch-level structures of a high temperature SiC NEMS-based FPGA.

III. High Temperature FPGA Architecture

A. Overall Architecture

For the proposed NEMS relay based high-temperature FPGA prototype, we adopt the island style FPGA architecture [11], the basic structure of which is shown in Fig. 2. As illustrated in the figure, three main building blocks of the

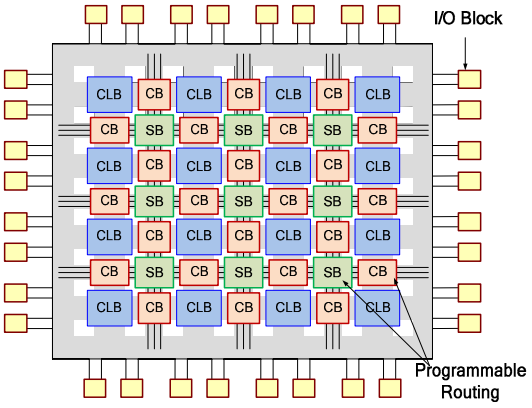

Figure 2. FPGA architecture consisting of interleaved configurable logic blocks (CLBs) and programmable interconnect (CB: Connection Box; SB: Switch Box).

FPGA prototype are Configurable Logic Block (CLB), Connection Box (CB) and Switch Box (SB). CLBs serve as the basic logic elements which can be configured to implement simple combinational or sequential logic functions, and CBs and SBs are two types of Programmable Interconnect (PI) which handle the FPGA routing. In particular, CBs form the interface between CLBs and the routing channels by creating connections between CLB inputs/outputs and routing tracks, while SBs form the programmable interconnect within the routing channels by connecting different routing wires at each intersection of a horizontal and vertical routing channel.

In order to understand the challenges of designing FPGA, we focus on the main building blocks for CLB and PI. Fig. 3 shows structures of the three building blocks. Each CLB contains a 7-input lookup table (LUT), a D flip-flop as the sequential element, and a MUX, which selects between the combinational and sequential outputs. Figure 3(b) depicts the symbol of a 4-terminal PI switch used for routing. One of the control terminals (B) is connected to ground and the other terminal (G) is connected to a configuration memory cell. When the control voltage is high, the switch turns on and presents a low resistance path between S and D. On the other hand, when the configuration cell stores '0', the routing switch is off and presents a high impedance path between the S and D terminals. We use bidirectional routing so that both CB (Fig. 3(c)) and SB (Fig. 3(d)) connections can be implemented with single NEMS switches. Although our FPGA prototype is a much simplified design compared to commercial FPGA, we choose the design parameters (e.g. number of CLBs and routing elements) according to Altera Stratix II family EP2S15F484C3 device, in order to get meaningful estimates of resource utilization for different benchmark circuits and for performance evaluation. Next, we describe the different SiC NEMS-based switch structures and use them to construct the building blocks of the FPGA.

B. NEMS switch structures and inverter design

Fig. 4 shows three SiC NEMS switch structures that we use to implement our FPGA building blocks. The switches are designed based on laterally actuated cantilever beams [4]. Fig. 4(a) shows the structure of a 3-terminal switch. The three terminals are Gate (G), Source (S) and Drain (D). The on/off state of the switch is determined by the electrostatic force between the gate electrode and the source i.e. the cantilever. When a voltage greater than the cantilever pull-in voltage (Vpull-in) is applied at G with respect to S, the consequential electrostatic force will pull the cantilever and cause it to move towards the gate electrode, eventually making the beam end touch D and forming a conducting channel between S and D. By sizing the beam/gate overlap and separation distance between beam/drain and beam/gate, it can be ensured that the beam never comes in contact with the gate, thus presenting large input impedance, similar in magnitude to the off-resistance of the switch.

Since the electrostatic force will pull the beam towards the drain irrespective of the polarity of the voltage difference between G and S, this 3-terminal switch can be used as a pull-up or pull-down switch by connecting the S terminal to VDD or VSS. Thus, it can be used to construct static CMOS-type logic gates, like the inverter described in [4]. G electrodes of both switches are connected together as the input and D electrodes are connected as output. When logic '0' (VSS) is applied at the input, the upper cantilever will be pulled-in to connect to D. The bottom cantilever will stay away from D under the repelling electrostatic voltage from G. As a result, D will have the same voltage as the upper relay after complete charging, meaning the output is logic '1'. Conversely, when logic '1' (VDD) is applied at the input, the bottom switch will turn on and discharge the output to logic'0'. The 3-terminal NEMS switch based inverters are used in both memory elements and D flip-flops in the proposed FPGA architecture.

Although the 3-terminal switch can be a building block for logic gates in static CMOS style, it would be redundant to configure multiple such switches into a single transmission gate or MUX, especially considering the large number of transmission gates and MUXes needed for constructing an FPGA. For this purpose, we can consider a 4-terminal and a 7-terminal NEMS switch using multilayer beams with separate control terminals and S/D terminals. Fig. 4(b) and (c) show these novel switch structures. In Fig. 4(b), the laterally actuated cantilever contains two layers. Main part of the cantilever is made of polycrystalline SiC, which is non-conducting. On the side wall of the cantilever, there are two conducting layers made of doped SiC, which are electrically isolated from each other. The left conducting layer denoted by 'B' (Beam), forms

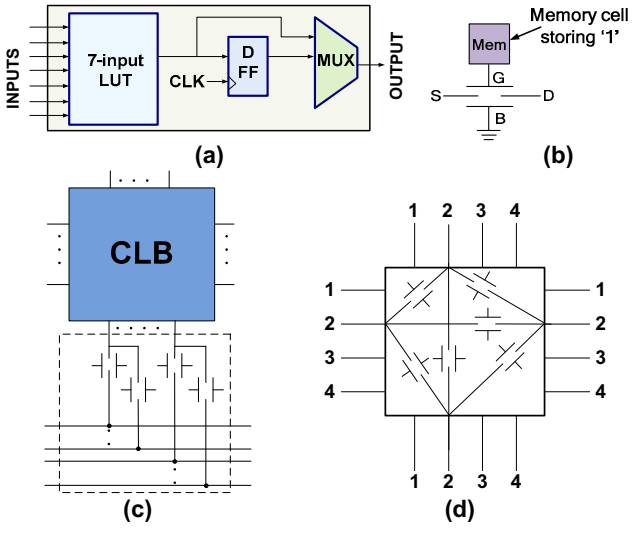

Figure 3. FPGA building blocks: (a) Configurable Logic Block (CLB); (b) PI routing switch; (c) Connection Box (CB); and (d) Switch Box (SB).

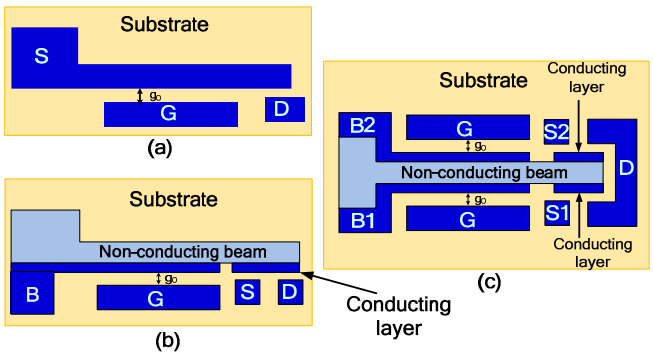

Figure 4. (a) 3-T NEMS single-layer switch; (b) 4-T NEMS multi-layer switch; (c) 7-T NEMS multi-layer switch for efficient implementation of 2x1 multiplexer.

the control terminal along with the G electrode, by forming a parallel-plate capacitor, whose voltage difference controls the movement of the cantilever. The right layer is a conducting channel to connect S and D terminals when the switch is in its on-state. Once the voltage difference between B and G goes above Vpull-in of the switch, the cantilever will move towards G electrode and form a connection between S and D, which can be removed simply by making V_{GB} zero. By attaching B to VSS or VDD, we get replacements for PMOS and NMOS pass transistors, without the associated degradation in voltage.

The 7-terminal switch works in the same way as the 4-terminal one. However, since there are electrodes and conducting layers on both side-walls of the cantilever, it has the flexibility to implement multiple functions using a single switch. The connection in Fig. 4(c) makes the 7-terminal switch act like a 2x1 MUX. Since in digital logic, G voltage could only be logic low or high, the cantilever gets pulled in towards one side only. The corresponding S value will get transmitted to D, which realizes the function of a MUX.

$$V_D = V_G \cdot V_{S1} + V_G' \cdot V_{S2} \quad (1)$$

C. *Building blocks*

The look-up tables (LUTs) are composed of 2^M memory elements which store the values corresponding to the truth-table of a mapped function and M-input multiplexers which choose the value from the appropriate memory element based on the input values. On the other hand, programmable interconnects in both CBs and SBs are implemented using four-terminal NEMS switches. Next, we describe the structure and functional behavior of the LUTs, D flip-flops and programmable interconnects based on the switch structures described the previous sub-section.

a) Look-up Table (LUT): A 7-input LUT is made up of 128 memory elements and a 128x1 MUX tree (see Fig. 5). The memory elements are SRAM-based storage cells constructed using a 4-terminal NEMS switch as a transmission gate for write access and two back-to-back 3-terminal NEMS switch based inverters, as shown in Fig. 5. During configuration, a voltage higher than the Vpull-in is applied to WE to turn on the 4-terminal switch for write access. Upon removal of the high voltage of WE, the switch will turn off and the value stored in the memory element will be held by the positive feedback loop formed by the two back-to-back inverters. Since read operations only happen after configuration, during which the stored value does not change, there is no need for a read access switch. The inverter is designed following a static CMOS style with two 3-terminal NEMS switches. The MUX is realized with multiple stages of 7-terminal multilayer NEMS relay. A switch-level symbol of the 2x1 MUX is also shown in Fig. 5, considering the 7-T switch as 2 connected 4-T switches.

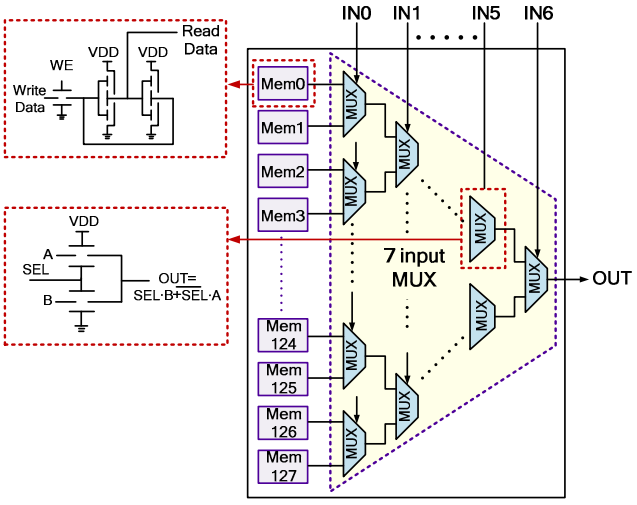

Figure 5. 7-input LUT with NEMS switch level schematic of the memory elements and the MUX tree.

b) D Flip-flop: NEMS D flip-flops are implemented using two cascading D latches in CMOS style (see Fig. 6). Each D-latch contains two 4-T NEMS switch based transmission gates and two back-to-back inverters. It is to be noted that we do not need a separate inverter for generating inverted version of CLK signal since the inverse polarity is achieved by connecting B electrode to VDD instead of VSS. The D flip-flop in Fig. 6 implements a positive-edge triggered master-slave structure.

c) Programmable Interconnect (PI): Each programmable interconnect component is realized using a 4-terminal NEMS switch (see Fig. 3(b) and Fig. 4(b)). One of the control terminals (B) is conncted to VSS and the gate (G) terminal is connected to the output of a configuration cell. When the cell stores logic '1', the routing switch turns on, and it turns off when the cell stores logic '0'.

IV. Simulation Results

A. *Switch Models*

Based on the behavior of NEMS cantilevers we fabricated, we electrically model the 3- and 4-terminal switches as shown in Fig. 7. In Fig. 7(a), C_{gs} is the parasitic capacitance between G and S. The distributed beam resistance is represented by two resistors of value $R_{beam}/2$. Resistance between S and D depends on the on-/off- state of the switch, which is determined by the voltage (V_{gs}) across C_{gs}. If $|V_{gs}|$ is less than Vpull-in, the switch is in its off-state. The open circuit between S and D can be modeled with an off resistance R_{off}, whose magnitude determines the leakage current flow through the gap due to tunneling effect. Based on the experimental result of the tunneling current provided in [4], we set R_{off} to be $10^{15}\Omega$. Once the cantilever is pulled-in, the switch is in its on-state and resistance between S and D is the contact resistance between beam end and D. This contact resistance is represented by R_{on} in the model, which is typically much larger than the beam resistance [4]. Therefore R_{sw} can be modeled as a voltage-controlled resistor.

Fig. 7(b) shows the model for the 4-terminal switch, for which R_{sw} is controlled by the voltage (V_{gb}) across capacitor

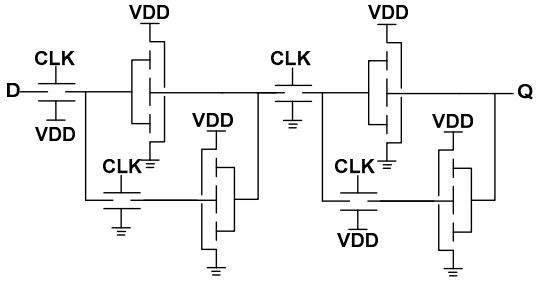

Figure 6. NEMS switch level schematic of a D flip-flop.

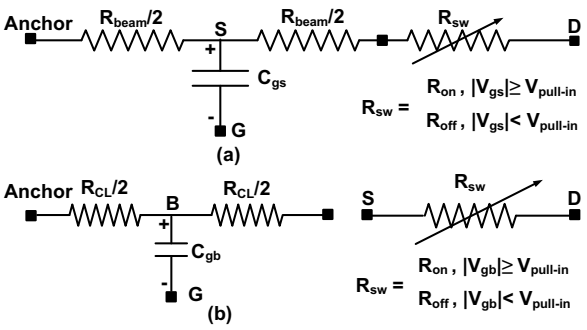

Figure 7. Electrical model of NEMS switch: (a) 3-terminal switch model; (b) 4-terminal switch model.

C_{gb}. Since V_{gb} is independent from the conducting channel between S and D, the R_{sw} is isolated from C_{gb}. R_{CL} models the resistance of the right conducting layer. Off-state resistance between S and D is R_{off} as before. On-resistance of a 4-terminal switch includes contact resistance of S and D, and resistance of the right conducting layer. The 7-terminal switch model consists of two 4-terminal models with proper terminal connections. Since we successfully fabricated 3-terminal SiC switches with beam length/width/thickness of 8µm/200nm/400nm and GS gap of 150nm, and proved their capability of operating for more than 21 billion cycles at room temperature, as well as 2 billion cycles for 500ºC, we use the fabricated device parameters as the basis of 3-T switch electrical modeling. For 4-terminal and 7-terminal switches, we designed switch dimensions based on the cantilever pull-in voltage equation [7] (W is total beam width and γ is ~0.25 for a cantilever), so that the pull-in voltage is below 5V. Other parameters of 4- and 7-terminal switches are calculated based on measured parameters of 3-terminal switches. Switch dimensions and modeling parameters are given in Table I.

For comparison, we also evaluate performance parameters of SiC based JFET-NEMS hybrid FPGA and CMOS FPGA, which, although works at room temperature, provides an general reference to show the advantages and disadvantages of two high-temperature FPGAs. JFET-NEMS hybrid FPGA contains SiC JFET-NEMS memory elements, D flip-flops, and NEMS MUX-tree as well as routing components. All JFET-based logic units are realized with JFET NOR gates, which are modeled according to fabricated devices, as in [12].

TABLE I. MODEL PARAMETERS OF NEMS SWITCHES

3-T switch Beam length/width/thickness	**8µm/200nm/400nm**
4-T switch Beam length/width(non-conducting layer)/thickness	**8.5µm/200nm/400nm**
3-T switch Gate to Source Gap	**150nm**
4-T switch Gate to Body Gap (g_0)	**90nm**
Conducting layer thickness	**150nm**
Gate Length	**7.5µm**
Left (Body)/right conducting layer length	**7.5µm/0.7µm**
SiC density	**3.33 g/cm^3**
Doped SiC resistivity	**0.05Ω·cm**
Young's modulus (E)	**330GPa**
Beam resistance for 3-T switch (R_{beam})	**25kΩ**
Resistance of the right conducting layer (R_{CL})	**3.1kΩ**
Cantilever contact resistance (R_{on})	**1MΩ**
Switch off resistance (R_{off})	**1PΩ**
GS (3-T switch)/GB (4-T switch) capacitance	**0.18fF/0.3fF**
3-T/4-T and 7-T switch (calculated) Vpull-in	**4.7V/4.32V**

B. Simulation Setup

Based on the above lumped electrical model of NEMS switches, we built HSPICE subcircuits for building blocks of both NEMS- and JFET-NEMS hybrid FPGAs. We use Altera Quartus II tool to map each of 6 ISCAS'85 and 8 ISCAS'89 benchmark circuits to Stratix II family EP2S15F484C3 device, which contains 12480 LUTs and registers. Then we extracted the RTL netlists with actual placement and routing information and mapped them to HSPICE netlists. Numbers of CBs and SBs of each mapped circuit were estimated based on the routing resource utilization information from Quartus II tools. In particular, we used supply voltage of 5V and +18V/-6V for NEMS-, JFET-NEMS FPGA, respectively. JFET-NEMS FPGA requires +18V/-6V supply voltages to achieve logic '1' of 6V and logic '0' of 0V, so as to be able to interface with NEMS MUX trees and routing elements. To provide a reference, we also obtained room temperature simulation results of CMOS FPGA (70nm Predictive Technology [13] and 1V supply), even though it is not a viable option for high-temperature applications. For the performance of both NEMS- and JFET-NEMS hybrid FPGAs, we extracted critical paths of benchmark circuits from Quartus II tool. We obtained critical path delays by taking into consideration both the electrical propagation delay and the mechanical switching delay. However, both delays are dominated by the mechanical delay (500 ns per switching based on measurement of our fabricated SiC NEMS switches). In addition, according to the dimensions of fabricated NEMS switch, JFET from [12] and 70nm transistors [13], we estimated the active area of the FPGAs.

C. Performance Estimate

Estimates of leakage current for the building blocks of three types of FPGAs are described in Table II, along with the overall leakage current, the configuration time and the total active area. From these results we can see that leakage current of NEMS FPGA at 500ºC is about 300,000X lower than that of CMOS FPGA at room temperature, due to the electromechanical nature of the NEMS switches. Since the scaling of NEMS switch is not subject to the limit of thermal voltage (K_BT/q), it is a promising option for ultra-low power high-temperature applications in terms of scalability. On the

TABLE II. LEAKAGE CURRENT, CONFIGURATION TIME AND AREA

Parameter	**Design Element**	**NEMS FPGA** 500ºC	**Hybrid FPGA** 500ºC	**CMOS FPGA** 25ºC
Leakage	7-input LUT	2.56pA	47.5mA	2.2µA
	D flip-flop	40.0fA	1.45mA	30.74nA
	Routing switch + Config. memory	25.0fA	25.0fA	1.0pA
	Entire FPGA	82.37nA	610.90A	27.84mA
Config. time	Entire FPGA	5.39s	189.31ms	191.27µs
Active area	Entire FPGA	66.58mm^2	129.45cm^2	0.30mm^2

TABLE III. COMPARISON OF DYNAMIC POWER AND CRITICAL DELAY OF ISCAS BENCHMARKS MAPPED TO THREE TYPES OF FPGAS

Circuit	Dynamic Power			Critical Path delay		
	NEMS FPGA (fJ/vec) 500°C	*Hybrid FPGA (nJ/vec) 500°C*	*CMOS FPGA (fJ/vec) 25°C*	*NEMS FPGA (µs) 500°C*	*Hybrid FPGA (µs) 500°C*	*CMOS FPGA (ns) 25°C*
c432	271	32.16	395	4.5	4.5	6.10
c1908	490	52.39	693	3.5	3.5	4.58
c3540	1268	111.61	1725	6.5	6.5	9.28
c5315	1394	153.50	1951	6.0	6.0	8.43
c6288	3080	301.13	4136	30.5	30.5	34.09
c7552	1748	209.74	2668	13.0	13.0	16.56
s838	399	32.40	551	3.5	3.5	3.12
s953	873	86.21	1223	1.5	1.5	1.87
s1196	791	81.18	1111	2.0	2.0	2.29
s1238	819	84.27	1150	2.0	2.0	2.34
s1423	945	76.77	1304	5.5	5.5	5.17
s1488	856	92.85	1207	1.5	1.5	1.81
s5378	2101	166.47	2896	1.5	1.5	1.51
s9234	1325	68.31	1787	3.0	3.0	3.22

other hand, JFET-NEMS FPGA exhibit huge leakage at high temperature due to the DC path from VDD to VSS, which is difficult to prevent due to the depletion mode JFET transistors. Considering the high supply voltage requirement for JFET circuits, the dynamic power is also very high and hence, total power consumption of JFET-NEMS hybrid FPGA may be unacceptable. Table II also shows the estimated total active area of three types of FPGAs, from which we can see the active area of NEMS FPGA is considerably larger than that of CMOS FPGA. In contrast, JFET-NEMS FPGA is also very inefficient in terms of area requirement since individual JFET transistors are very large (W/L=100µm/10µm [12]). Table III shows the comparison of transition energy per vector and performance (in terms of critical path delay) for different ISCAS benchmark circuits for the NEMS FPGA and the hybrid FPGA. Corresponding values for CMOS FPGA at room temperature are presented for reference. The results show that transition energy of NEMS FPGA is comparable to that of CMOS FPGA (note the larger units for hybrid FPGA). When it comes to performance, both NEMS- and JFET-NEMS hybrid FPGA exhibit relatively larger propagation delay compared to CMOS FPGA, which is mainly contributed by the mechanical transition delay. The large switching delay also leads to large configuration time for NEMS FPGA. However, with appropriate design of the SiC NEMS devices, it is possible to achieve ~1GHz operating frequency [14]. Table IV summarizes the observations based on our simulation results. The NEMS FPGA outperforms the hybrid FPGA in terms of power and area, and has comparable read/write performance and stability.

V. CONCLUSION

We have presented a reconfigurable computing platform for high temperature operation using nanoscale electromechanical switch fabric. The target operating temperature (>500°C) is appropriate for many industrial, automotive and space applications. Although the proposed platform follows a conventional FPGA architecture, high temperature operation is

TABLE IV. COMPARISON OF PERFORMANCE METRICS

Metric / FPGA Type	Power	Performance		Active area	High-T (>500°C) Capable?
		Read Time	*Write Time*		
Hybrid FPGA	High	High	Moderate	Large	YES
NEMS FPGA	Low	High	High	Small	YES
CMOS FPGA	Moderate	Good	Low	Small	NO

enabled through appropriate choice of material (SiC) and switch (NEMS) fabric. We have presented a novel multi-layer NEMS switch structure for efficient implementation of the mux-trees and memory elements. We have fabricated the basic NEMS switches using SiC beams with nanoscale geometry and measured relevant switch parameters. Using the measured values from these switches, we have shown that an all-mechanical SiC FPGA is significantly more power/performance/area efficient than an alternative JFET-NEMS hybrid FPGA realization. It also shows several orders of magnitude less leakage at high temperature than CMOS FPGA at room temperature. High-temperature electronics such as microcontrollers would typically need to operate at hundreds of KHz to tens of MHz frequency. At this speed, it is sufficient for the NEMS switches to reliably operate for 10^{11}-10^{13} cycles for an acceptable lifetime of 5-10 years. Our fabricated switches have been demonstrated to operate reliably over 23 billion cycles at 500°C. With tuning of switch design and improvement in nanolithography, we believe, it is very much possible to achieve the target device lifetime along with improvement in integration density and performance.

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